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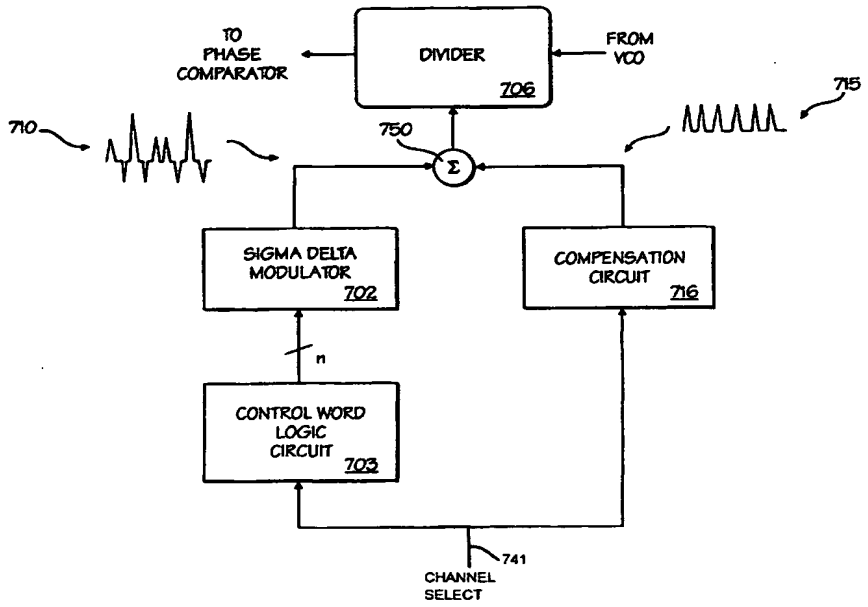
(54) Title: METHOD AND APPARATUS FOR A FREQUENCY SYNTHESIZER HAVING A COMPENSATED SIGMA DELTA MODULATOR OUTPUT SIGNAL




(57) Abstract: A method is described that involves combining (750) a sigma delta modulator output signal (710) with a second signal (715) to form a third signal that controls the division performed by a divider (706). An apparatus that can execute the method is also described.

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# Method and Apparatus For A Frequency Synthesizer Having A Compensated Sigma Delta Modulator Output Signal

The present application hereby claims the benefit of the filing date of a related Provisional Application entitled filed September 27, 1999, and assigned Application Serial No. 60/156,228.

## FIELD OF THE INVENTION

The field of invention relates generally to wireless signal reception and transmission; more specifically the invention relates to reducing jitter from Fractional N synthesis.

## BACKGROUND

Super Heterodyne and Frequency Shift Keyed (FSK) Modulation/Demodulation

Figure 1 shows a portion 106 of a receiving device 166 referred to as a demodulator. A demodulator 106 provides a signal (commonly referred to as a baseband signal b(t) in various applications) that is representative of the information being sent from a transmitting device 165 to a receiving device 166. The demodulator 106 extracts (i.e., demodulates) the baseband signal b(t) from a high frequency wireless signal that "carries" the baseband signal b(t) through the medium (e.g., airspace) separating the transmitting and receiving devices 165, 166.

The particular demodulator 106 example of Figure 1 is designed according to: 1) a demodulation approach that is commonly referred to as super heterodyne detection (hereinafter referred to as a heterodyne detection for simplicity); and 3) a modulation/demodulation scheme referred to as Frequency Shift Keying (FSK). The industry standard referred to as "BLUETOOTH" (the requirements of which may be found in "Specification of the Bluetooth System",

Core v.1.0B, 12/1/99, and published by the Bluetooth Special Interest Group (SIG)) can apply to both of these approaches and, accordingly, will be used below as a basis for reviewing the following background material.

Heterodyne detection is normally used when dedicated channels are allocated within a range of frequencies 111 (where a range of frequencies may also be referred to as a "band" 111). For BLUETOOTH applications within the United States, 89 channels $110_1$, $110_2$, $110_3$, . . . $110_{79}$ are carried within a 2.400 GHz to 2.482 GHz band 111. Each of the 79 channels are approximately 1 Mhz wide and are centered at frequencies 1 Mhz apart.

The first channel $110_1$ is centered at 2.402 Ghz, the second channel $110_2$ is centered at 2.403 Ghz, the third channel $110_3$ is centered at 2.404 Ghz, etc., and the seventy ninth channel $110_{79}$ is centered at 2.480 Ghz. The heterodyne demodulator 106 accurately receives a single channel while providing good suppression of the other channels present within the band 111. For example, if channel $110_2$ is the channel to be received, the baseband signal b(t) within channel $110_2$ will be presented while the baseband signals carried by channels $110_1$, and $110_3$ through $110_{79}$ will be suppressed.

An FSK modulation/demodulation approach is commonly used to transmit digital data over a wireless system. An example of an FSK modulation approach is shown in Figure 1. A transmitting modulator 105 within a transmitting device 165 modulates a baseband signal at a carrier frequency $f_{carrier}$ into an antennae 102. That is (referring to the frequency domain representation 150 of the signal launched into the antennae 102) if the baseband signal corresponds to a first logic value (e.g., "1"), the signal 150 has a frequency of $f_{carrier}$+ fo. If the data to be transmitted corresponds to a second logic value (e.g., "0"), the signal has a frequency of $f_{carrier}$ - fo.

Thus, the signal launched into the antennae 102 alternates between frequencies of $f_{carrier}$+ fo and $f_{carrier}$ –fo depending on the value of the data being transmitted. Note that in actual practice the transmitted signal 150 may have a profile 151 that is distributed over a range of frequencies in order to prevent

large, instantaneous changes in frequency. The carrier frequency $f_{carrier}$ corresponds to the particular wireless channel that the digital information is being transmitted within. For example, within the BLUETOOTH wireless system, $f_{carrier}$ corresponds to 2.402 Ghz for the first channel $110_1$. The difference between the carrier frequency and the frequency used to represent a logical value is referred to as the deviation frequency fo.

Referring now to the heterodyne demodulator 106, note that the signal received by antennae 103, may contain not only every channel within the frequency band of interest 111, but also extraneous signals (e.g., AM and FM radio stations, TV stations, etc.) outside the frequency band 111. The extraneous signals are filtered by filter 113 such that only the frequency band of interest 111 is passed. The filter 113 output signal is then amplified by an amplifier 114.

The amplified signal is directed to a first mixer 116 and a second mixer 117. A pair of downconversion signals d1(t), d2(t) that are 90° out of phase with respect to each other are generated. A first downconversion signal d1(t) is directed to the first mixer 116 and a second downconversion signal d2(t) is directed to the second mixer 117. Each mixer multiples its pair of input signals to produce a mixer output signal. Note that the transmitting modulator 105 may also have dual out of phase signals that are not shown in Figure 1 for simplicity. Transmitting a pair of signals that are 90° out of phase with respect to one another conserves airborne frequency space by a technique referred to in the art as single sideband transmission.

The frequency $f_{down}$ of both downconversion signals d1(t), d2(t) is designed to be $f_{carrier} - f_{IF}$. The difference between the downconversion frequency $f_{down}$ and the carrier frequency $f_{carrier}$ is referred to as the intermediate frequency $f_{IF}$. Because it is easier to design filters 118a,b and 127a,b that operate around the intermediate frequency, designing the downconversion that occurs at mixers 116, 117 to have an output term at the intermediate frequency $f_{IF}$ enhances channel isolation.

The mixer 117 output signal may be approximately expressed as

$$kb_{FSK}(t)\cos(2\pi f_{carrier} t)\cos(2\pi f_{down} t). \quad \text{Eqn. 1}$$

Note that Equation 1 is equal to

$$kb_{FSK}(t)[\cos(2\pi (f_{carrier} - f_{down})t)+\cos(2\pi (f_{carrier}+f_{down})t)] \quad \text{Eqn. 2}$$

which is also equal to

$$kb_{FSK}(t)\cos(2\pi f_{IF} t) + kb_{FSK}(t)\cos(2\pi (f_{carrier}+f_{down})t) \quad \text{Eqn. 3}$$

using known mathematical relationships. The $b_{FSK}(t)$ term represents a frequency shift keyed form of the baseband signal (e.g., a signal that alternates in frequency between +fo for a logical "1" and –fo for a logical "0"). The constant k is related to the signal strength of the received signal and the amplification of amplifier 114. For approximately equal transmission powers, signals received from a nearby transmitting device are apt to have a large k value while signals received from a distant transmitting device are apt to have a small k value.

Equation 3 may be viewed as having two terms: a lower frequency term expressed by $kb_{FSK}(t)\cos(2\pi f_{IF} t)$ and a higher frequency term expressed by $kb_{FSK}(t)\cos(2\pi (f_{carrier}+f_{down})t)$. Filter 118b filters away the high frequency term leaving the lower frequency term $kb_{FSK}(t)\cos(2\pi f_{IF} t)$ to be presented at input 119 of amplification stage 125. Note that, in an analogous fashion, a signal $kb_{FSK}(t)\sin(2\pi f_{IF} t)$ is presented at the input 126 of amplification stage 170.

Amplification stage 125 has sufficient amplification to clip the mixer 117 output signal. Filter 127b filters away higher frequency harmonics from the clipping performed by amplification stage 125. Thus, amplification stage 125 and filter 127b act to produce a sinusoidal-like waveform having approximately uniform amplitude for any received signal regardless of the distance (e.g., k factor) between the transmitting device and the receiving device.

After filter 127, a signal s(t) corresponding to $Ab_{FSK}(t)\cos(2\pi f_{IF} t)$ is presented to the frequency to voltage converter 128 input 129 (where A reflects the uniform amplitude discussed above). The spectral content S(f) of the signal s(t) at the frequency to voltage converter 128 input 129 is shown at Figure 1. The signal s(t) alternates between a frequency of $f_{IF}$ + fo (for a logical value of "1")

and a frequency of $f_{IF}$ – fo (for a logical value of "0"). The spectral content S(f) of the signal s(t) at the frequency to voltage converter 128 input 129 is mapped against the transfer function 160 of the frequency to voltage converter 128 in order to reproduce the baseband signal b(t) at the demodulator output.

Frequency Synthesis

Referring back to the pair of downconversion signals d1(t), d2(t) that are directed to mixers 116, 117, recall that the downconversion signals d1(t) and d2(t) should have a downconversion frequency $f_{down}$ equal to $f_{carrier}$ -$f_{IF}$ for each of the channels $110_1$ through $110_{79}$. For example, for an intermediate frequency $f_{IF}$ of 3Mhz, the frequency synthesizer 140 is responsible for generating a frequency of 2.399 Ghz in order to receive the first channel $110_1$ (i.e, $f_{carrier}$ -$f_{IF}$ = 2.402 – 0.003 Ghz = 2.399Ghz); a frequency of 2.400 Ghz in order to receive the second channel $110_2$; a frequency of 2.401 Ghz in order to receive the third channel $110_3$; . . . etc., and a frequency of 2.477 Ghz in order to receive the 79th channel $110_{79}$. A channel select input 141 presents an indication of the desired channel to the frequency synthesizer 140.

Both the transmitting device 165 and the receiving device 166 typically have a frequency synthesizer. A frequency synthesizer 140 is shown in the receiving device 166 (but not the transmitting device 165 for simplicity). Frequency synthesizers typically create their output signals by multiplying a reference frequency (such as the frequency of a local oscillator). As seen in Figure 1, frequency synthesizer 140 multiplies the frequency of local oscillator 142 to produce downconversion signals d1(t) and d2(t). For example, for a local oscillator 142 reference frequency of 13.000 MHz, frequency synthesizer 140 should have a multiplication factor of 184.53846 to produce downconversion signals d1(t), d2(t) used to receive the first channel $110_1$ (i.e., 184.53846 x 13.000MHz = 2.399 GHz).

A problem with wireless technology involves jitter in the frequency synthesizer 140 output. Jitter is the inability of the frequency synthesizer 140 to

produce downconverting signals d1(t), d2(t) with a stable frequency. That is, the downconversion frequency $f_{down}$ "jitters" about, rather than remains fixed at, the correct downconversion frequency for the applicable channel. As the downconversion frequency $f_{down}$ of the synthesizer 140 increasingly varies about its ideal value, increased distortion is observed in the baseband signal b(t) at the output of the demodulator 106.

Figure 2a shows the demodulator 106 output signal 250 if the downconversion frequency is ideal. As discussed above, the spectral content 253 of the ideal signal $k*b_{FSK}(t)\cos(2\pi f_{IF}t)$ produced by filters 127a,b will be centered at the intermediate frequency $f_{IF}$. Since the origin 251 of the voltage to frequency converter 128 transfer curve 260 is centered at the intermediate frequency $f_{IF}$, the output signal 250 will have both no offset and equal amplitude swings 252a, 252b.

Variation (i.e., jitter) in the downconversion frequency $f_{down}$, however, will cause the spectral content 254 of the signal produced by filters 127a,b to be centered at a wavering offset 255 from the ideal intermediate frequency $f_{IF}$. That is, because $f_{IF}$ in equation 3 corresponds to $f_{carrier} - f_{down}$, if $f_{down}$ wavers, the value of $f_{IF}$ in equation 3 will not be fixed at (but rather vary about) the ideal $f_{IF}$ value that is centered at the origin of the voltage to frequency converter 128 transfer curve 260. As such, the output signal 258 produced by the demodulator will have a time varying offset 256 (commonly referred to as baseline wander) and may even exhibit moments of unequal amplitude swing 257a,b (when the offset 256 is large enough).

**SUMMARY OF INVENTION**

A method that comprises combining a sigma delta modulator output signal with a second signal to form a third signal that controls the division performed by a divider.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not limitation, in the Figures of the accompanying drawings in which:

**Figure 1** shows a depiction of a wireless transmission system.

**Figure 2** shows signals that may be produced by the wireless transmission system of Figure 1.

**Figure 3** shows an embodiment of a frequency synthesizer.

**Figures 4** shows an embodiment for a wireless sub band.

**Figure 5a** shows a higher frequency sigma delta modulator output signal.

**Figure 5b** shows a lower frequency sigma delta modulator output signal.

**Figure 6a** shows a divider output signal and phase comparator output signal that result from a higher frequency sigma delta modulator output signal.

**Figure 6b** shows a divider output signal and phase comparator output signal that result from a lower frequency sigma delta modulator output signal.

**Figure 7** shows an embodiment of a portion of a frequency synthesizer circuit having reduced jitter.

**Figure 8** shows an embodiment of wireless sub band approach that may be used with the circuit of Figure 7.

**Figure 9** shows a more detailed embodiment of a portion of a frequency synthesizer circuit having reduced jitter.

**Figure 10** shows a method that may be executed with the frequency synthesizer embodiments of Figures 7 and 9.

## DETAILED DESCRIPTION

A method is described that comprises combining a sigma delta modulator output signal with a second signal to form a third signal that controls the division performed by a divider. An apparatus that can execute the method is also described.

Another method is described that comprises generating a sigma delta modulator output signal having an incorrect average value for a desired channel. A correct average value for the desired channel has a first offset from a nearest output value of the sigma delta modulator. The incorrect average value has a second offset from the nearest output value of the sigma delta modulator such that first offset is less than said second offset. The method further comprises combining the sigma delta modulator output signal having the incorrect average value with a compensation signal. The compensation signal has an average value that compensates for the incorrect average value so that a signal having the correct average value for the desired channel is produced. An apparatus that can execute the method if also described.

Another method is described that comprises generating a sigma delta modulator output signal having an incorrect average value for a desired channel. The sigma delta modulator output signal has a greater frequency than a sigma delta modulator output signal having a correct average value for the desired channel. The method further comprises combining the sigma delta modulator output signal with a compensation signal. The compensation signal has an average value that compensates for the incorrect average value so that a signal having the correct average value for the desired channel is produced. An apparatus that can execute the method is also described.

These and other methods, along with the apparati that can execute them are discussed in more detail below.

Downconverting is the act of reducing or eliminating the frequency of a first signal that is carrying a second signal. Referring back to Figure 1, as an

example, note that the downconversion signals d1(t), d2(t) reduce the carrier frequency of the FSK modulated baseband signal $b_{FSK}(t)$ from $f_{carrier}$ to $f_{carrier} - f_{down}$. A downconversion frequency is a frequency that subtracts from the frequency of the first signal mentioned just above.

Figure 3 shows an exemplary frequency synthesizer 340 embodiment. A frequency synthesizer 340 may be formed by coupling a sigma delta modulator 302 to a divider 306 that is located within the feedback path of a phase lock loop (PLL) circuit 301. The PLL circuit 301 is used to effectively multiply the frequency of a reference frequency (such as the frequency of a signal from a local oscillator 342 or other frequency reference). As developed in more detail below, the PLL 301 output signal (which is the signal appearing at the output of the voltage controlled oscillator (VCO) 307) has a frequency ($f_{VCO}$) that is a multiple ($N_{AVE}$) of the local oscillator 342 frequency (fosc). That is, $f_{VCO} = N_{AVE} \cdot fosc$.

In the depiction of Figure 3, the frequency of the synthesizer output 371 signal is the downconversion frequency $f_{down}$ referred to in the background. Note that in the embodiment of Figure 3, a frequency factor 370 is located between the output of the VCO 307 and the output 371 of the synthesizer 340. The frequency factor 370 allows the VCO 307 to operate at a lower frequency than the downconversion frequency $f_{down}$. Thus, for the embodiment of Figure 3 where the frequency factor 370 doubles its input frequency, $f_{down} = 2f_{VCO}$. Whether or not the VCO 307 output signal should be factored by 2 or another value (or at all) is a decision made by the designer in light of the particular application the synthesizer 340 is directed to.

As a practical example, recalling from the discussion in the background that a synthesizer 340 multiplication factor of 184.53846 can be used to produce a 2.399GHz downconversion frequency for the first BLUETOOTH channel $110_1$ for a local oscillator 342 frequency of 13.000 MHz; note that the use of the doubling frequency factor 370 allows the multiplication performed by the PLL 301(i.e., $N_{AVE}$) to be 92.26923 (i.e., 92.26923 x 2 = 184.53846). This also corresponds to a VCO 307 output signal frequency $f_{VCO}$ of 1.1995 Ghz.

The frequency $f_{VCO}$ of the VCO 307 output signal is divided within the feedback path of the PLL 301 by a divider 306. A divider 306 is a circuit that emits an output signal having a reduced frequency as compared to its input signal. Divider 306 allows the VCO 307 to operate at a higher frequency than the local oscillator 342 (which effectively provides the desired frequency multiplication performed by the PLL circuit 301). The divider 306 is typically a counter-like circuit that triggers an edge at its output signal after a number of edges are observed in the VCO 307 output signal.

The degree to which the frequency is reduced is referred to as the division or the division factor. Dividers have a second input used to control the division performed by the divider. A divider's division factor "N", will vary (as discussed in more detail further ahead) depending upon the sigma delta modulator 302 output value. Over the course of time in which a constant $f_{VCO}$ is produced, at one instance the division factor may be "N" while at another instance it may be "N-1". Thus, as explained in more detail below, the division factor N varies even if a constant $f_{VCO}$ is desired.

Given that the division factor N varies, the average division factor realized over time ($N_{AVE}$) corresponds to the multiplication performed by the PLL 301. That is, the average frequency of the divider 306 output signal is $f_{VCO}/N_{AVE}$. Phase comparator 309 produces an output based upon the phase difference between the divider 306 output signal and the local oscillator 342 signal. The phase comparator 309 output is effectively integrated or averaged by loop filter 310 (via charge pump 311) which produces the loop filter 310 output voltage that is presented to the VCO 307 input. The VCO 307 output signal frequency $f_{VCO}$ is proportional to the voltage placed at the VCO 307 input.

Ideally, the loop filter 310 output voltage becomes stable (i.e., fixed or "locked") when the frequency of the local oscillator fosc becomes equal to $f_{VCO}/N_{AVE}$; that is, when the VCO 307 output frequency $f_{VCO}$ becomes equal to $N_{AVE}$·fosc. Thus, in this manner, the PLL circuit 301 effectively multiplies the frequency of the local oscillator 342 by a factor of $N_{AVE}$. Frequency synthesis performed

according to the technique described above (i.e., modulating the division performed by a divider in a PLL feedback path) is commonly referred to as Fractional-N (or N-Fractional) synthesis.

Note that the proper value of $N_{AVE}$ for each application will depend upon the wireless system being implemented and the local oscillator 342 frequency employed. Other BLUETOOTH related embodiments may employ different local oscillator values (e.g., 8.000MHz) which will affect the average division factor $N_{AVE}$. Furthermore, wireless approaches other than BLUETOOTH (e.g., HomeRF, IEEE 802.11, GSM, Digitally Enhanced Cordless Telephony (DECT), etc.) which may employ different downconversion frequencies than those employed by BLUETOOTH may implement their own particular combination of local oscillator 342 frequencies and/or average divider factors $N_{AVE}$.

In the embodiment of Figure 3, a static control word logic circuit 303 is used to translate an indication of the desired channel (presented at the channel select input 341) into a control word (having n bits) that is submitted to the sigma delta modulator 302 input. That is, each channel has an associated, fixed control word value. A unique sigma delta modulator output signal is created for each unique control word value that is presented by the static control word logic circuit 303.

Sigma delta modulators are a class of circuit known in the art that craft an output having a beneficial spectral shape (e.g., by describing an input signal with higher frequencies than those emphasized by the input signal). More details concerning sigma delta modulators (which may also be referred to as delta sigma modulators) and their use in Fractional N synthesis may be found in "A Multiple Modulator Fractional Divider", B. Miller and R.J. Conley, IEEE Transactions on Instrumentation and Measurement, vol. 40, no. 3, June 1991.

The sigma delta modulator 302 output signal 373 (which may also be referred to as the modulator output signal, modulator output pattern and the like) controls the average division $N_{AVE}$ performed by divider 306 and, in so doing, controls the frequency multiplication performed by the PLL circuit 301.

Because the frequency multiplication performed by the PLL 301 determines the PLL's output frequency $f_{VCO}$; and because the PLL output frequency $f_{VCO}$ affects the value of the downconversion frequency $f_{down}$, the sigma delta modulator 302 output signal 373 is used to control which channel is demodulated.

The sigma delta modulator 302 output signal 373 is a sequence of random or pseudo random values. An example of a sigma delta modulator 302 output signal 373 having four discrete output values (–1, 0, +1 and +2) is shown in Figure 3. Other output values are possible. The number of output values typically depends upon the order of the sigma delta modulator .

The sigma delta modulator embodiment 302 of Figure 3 can produce signals having four discrete output values: –1, 0, +1 and +2. The corresponding divider 306 has four discrete division factors: N-1; N; N+1; and N+2. Each of the different division factors may be used to divide the frequency of the VCO output signal. For example, if N of the divider 306 is configured to be equal to 92, the divider 306 is designed to divide at factors of 91, 92, 93 and 94. Thus, if the sigma delta modulator 302 output is –1 the division factor is N-1 (e.g., 91); if the sigma delta modulator 302 output is 0 the division factor is N (e.g., 92); if the sigma delta modulator 302 output is +1 the division factor is N+1 (e.g., 93); and if the sigma delta modulator 302 output is +2 the division factor is N+2 (e.g., 94).

Figure 4 shows an exemplary embodiment of a BLUETOOTH receiver design having: 1) a divider 306 with an N of 92; 2) a local oscillator 342 having a frequency $f_{OSC}$ of 13.000 MHz; 3) a 2.0 frequency factor 370 between the VCO 307 output and the synthesizer output 371; and 4) an intermediate frequency $f_{IF}$ of 3.000MHz. Figure 4 shows a listing of (for each of a sampling of channels): 1) the average value of the sigma delta modulator 302 output signal $SDO_{AVE}$ (which is discussed in more detail below); 2) the average division factor $N_{AVE}$ of the divider 306 (which is equal to the multiplication performed by the PLL circuit 301 as discussed above); 3) the VCO 307 output signal frequency $f_{VCO}$; 4) the downconversion frequency $f_{down}$ (i.e., the synthesizer 340 output signal frequency); and 5) the carrier frequency $f_{carrier}$ (which is equal to $f_{down} + f_{IF}$ as

discussed in the background). The divider 306 used for the embodiment of Figure 4 has divider factors of 91/92/93/94 (i.e., N=92 over N-1/N/N+1/N+2) for the corresponding sigma delta modulator 302 output values of –1/0/+1/+2.

Recall that the sigma delta modulator 302 output (which is responsive to the control word that is produced by the static control word logic circuit 303) controls the average division factor $N_{AVE}$ of the divider 306; and, in so doing, controls the frequency multiplication performed by the PLL circuit 301. For each control word (i.e., for each channel select value 341), the sigma delta modulator 302 will produce a sequence of values having an overall average value that corresponds to the division factor $N_{AVE}$ used to select the appropriate channel.

The average value of the sigma delta modulator output signal, $SDO_{AVE}$, is the average of the values observed in the sigma delta modulator 302 output signal for a particular control word. $SDO_{AVE}$, may therefore be expressed as:

$$SDO_{AVE} = (1/m)\sum SDO(T) \qquad \text{Eqn. 4}$$

where: 1) SDO(T) is the sequence of sigma delta modulator output values; and 2) m is the number of number of sigma delta modulator output values within the sequence SDO(T). For example, if a sigma delta modulator output signal continually repeats the sequence: –1, +2, 0, +1, 0 +2, +1, 0, +1, -1; an $SDO_{AVE}$ of 0.500 results because the sum of all the values in the sequence is +5 and there are ten values within the repeated sequence (i.e., 5/10=0.500). Note that the sequence may appear as a multileveled output signal (such as signal 373 of Figure 3) or as a binary encoded signal (e.g., corresponding to the above sequence: 101, 010, 000, 001, 000, 010, 001, 000, 001, 101 where the highest order bit is a polarity bit).

Consistent with the design embodiment discussed above (where a sigma delta output value of 0 corresponds to a division factor of N) the sigma delta modulator output signal example provided above will continually vary the

division factor (within the PLL feedback loop) according to N-1, N+2, N, N+1, N, N+2, N+1, N, N+1, N-1. Straightforward mathematical derivation will show that a sigma delta modulator output signal having an average value $SDO_{AVE}$ as provided in Equation 4 above will cause the divider 306 to have an average division factor $N_{AVE}$ of:

$$N_{AVE} = N + SDO_{AVE} \qquad \text{Eqn. 5}$$

where a sigma delta modulator output value of 0 corresponds to a division factor of N. Thus, referring to Figure 4, note that the values listed for $N_{AVE}$ are the value of N for the particular embodiment (i.e., 92) added to the values listed for $SDO_{AVE}$.

Note that the embodiment of Figure 4 uses a sub-band approach. In a sub-band approach, a portion (rather than the entirety) of the range of potentially desirable channels (e.g., channel $110_1$ through channel $110_{79}$) is demodulated with sigma delta modulator signals having an $SDO_{AVE}$ between neighboring sigma delta modulator output values. For example, as seen in Figure 4, only channels 1 through 20 are demodulated with an $SDO_{AVE}$ between 0 and +1 inclusive. Thus channels 1 through 20 form a sub-band within the frequency band of interest.

The entire range of channels are made available by combining sub-bands. For example, with respect to the embodiment of Figure 4, channels 21 through 41 may be allocated within one or more other sub-bands. The channels within these other sub-bands may be demodulated, as just a few of many possible approaches, with sigma delta modulator output signals having an $SDO_{AVE}$ between another pair of sigma delta modulator output values (e.g., between +1 and +2 for the embodiment of Figure 4); or changing the division factor of the divider (e.g., changing from N=92 to N=93) or a combination of both. Whether or not a sub-band approach is to be used and which type of sub-band approach

should be used are decisions a designer can make in light of the constraints associated with his/her particular application.

Recall from above that for each control word (i.e., for each channel select value 341), the sigma delta modulator 302 will produce an output signal sequence having a particular $SDO_{AVE}$. For each channel select value 341, the static control word logic circuit 303 presents a control word to the sigma delta modulator for the particular desired channel. The static control word logic circuit 303 may be implemented as a look up table that converts a given channel select value into the proper control word or a logic circuit that calculates the proper control word partially based upon Equation 6 which is described below.

The average value of the sigma delta modulator output signal (for a particular input control word provided by the static control word logic circuit 303) may be expressed as:

$$SDO_{AVE} = CW/CW_{modulo} \qquad \text{Eqn. 6}$$

where CW is the value of the control word provided by the static control word logic circuit 303 (e.g., any binary word having a base ten value between 0 and 2048 inclusive for an eleven bit control word) and $CW_{modulo}$ is the modulo of the control word provided by the static control word logic circuit 303 (e.g., $2^{11} = 2048$ for an eleven bit control word). Thus, for an eleven bit control word having a base ten value of 551, a sigma delta modulator will produce an $SDO_{AVE}$ of $551/2048 = 0.2690$. Given that $f_{VCO} = N_{AVE} \cdot fosc$, Equations 5 and 6 may be used to describe the VCO frequency as a function of the control word. That is,

$$f_{VCO} = fosc(N + CW/CW_{modulo}) \qquad \text{Eqn. 7}$$

Figures 5a and 5b show examples of two different sigma delta modulator output signals. Figures 5a and 5b were both generated with a 2nd order sigma delta modulator. The $SDO_{AVE}$ for the sigma delta modulator output signal 501 of Figure 5a is approximately 0.500 which, referring to Figure 4, corresponds to channel 7 (i.e., $f_{carrier} = 2.408$ GHz). The $SDO_{AVE}$ for the sigma delta

modulator output signal 502 of Figure 5b is approximately 1.000 which, referring to Figure 4, corresponds to channel 20.

Because the sigma delta modulator uses a clock signal to generate signals 501, 502 of Figures 5a and 5b, the smallest available amount of time over which the output signal can change corresponds to the clocking period $\Delta t_{505}$ of the sigma delta modulator. The clocking period $\Delta t_{505}$ may also be referred to as the resolution period of the sigma delta modulator output signal. The resolution period $\Delta t_{505}$ shown in Figure 5a is the same resolution period that applies to Figure 5b.

Comparing the sigma delta modulator output signal 501 of Figure 5a with the sigma delta modulator output signal 502 of Figure 5b, note that the sigma delta modulator output signal 501 of Figure 5a is a higher frequency signal than the sigma delta modulator output signal 502 of Figure 5b. Indicia of a first signal being a higher frequency signal than a second signal include: 1) more changes per unit of time exhibited by the first signal; and/or 2) more abrupt change in output signal value per unit of time exhibited by the first signal. A detailed discussion of these indicia for signals 501 and 502 is appended at the end of this detailed description.

Sigma delta modulator output signals become lower in frequency as the $SDO_{AVE}$ value of the signal approaches one of the discrete sigma delta modulator output values. Thus, sigma delta modulator output signal 501 is a higher frequency signal than sigma delta modulator output signal 502 because the $SDO_{AVE}$ of signal 501, being approximately 0.500, is remote from output values 0 and +1 (as well as –1 and +2); while the $SDO_{AVE}$ value of signal 502, being 1.000, approaches the sigma delta modulator output value of +1.

As the $SDO_{AVE}$ value of a sigma delta modulator output signal approaches a discrete output value of the sigma delta modulator, the sigma delta modulator is able to produce an accurate signal (i.e., an accurate $SDO_{AVE}$ value) by inserting a disproportionate share of values in the output signal sequence that are equal to the approached sigma delta modulator output value. For example, as seen in

Figure 5b, signal 502 has a disproportionate share of output values equal to +1. This results in the signal having fewer changes per unit of time; and/or less abrupt change in output signal value per unit of time.

Referring briefly back to Figure 3, it has been discovered that more jitter is produced in the frequency of the VCO 307 output signal as the $SDO_{AVE}$ of the sigma delta modulator output signal approaches an output value of the sigma delta modulator. Stated another way, higher frequency sigma delta modulator output signals produce less jitter in the VCO 307 output signal than lower frequency sigma delta modulator output signals. It has been observed, therefore, that sigma delta modulator output signal 502 creates more jitter in the VCO 307 output frequency than sigma delta modulator output signal 501. In the design embodiment of Figure 4, this corresponds to more baseline wander (as shown back in Figure 2b) observed for channel 20 than for channel 0.

Insight into why the frequency of the sigma delta modulator output signal will affect jitter in the frequency of the VCO 307 output signal is presented in Figure 6a, Figure 6b and the following discussion. The discussion concerning Figures 6a and 6b relates to the mechanism by which the presence of consecutive, equal output values in the sigma delta modulator output sequence will be transformed into jitter. However, it is to be understood that the jitter causing mechanism(s) of all of the indicia discussed above operate similar to that discussed below.

Figure 6a shows an exemplary portion of a 0, +1, 0, +1 sigma delta modulator output signal 601 and Figure 6b shows an exemplary portion of a 0, +1, +1, 0 sigma delta modulator output signal 602. Sigma delta modulator output signal 602, having consecutive, equal values of +1, +1, changes the division performed by the divider less frequently in time period 650 than sigma delta modulator output signal 601which does not have consecutive, equal values.

A pair of corresponding, exemplary divider output signals for each of the sigma delta modulator signals 601, 603 is also shown in Figures 6a and 6b

Figure 6a shows the divider output signal 603 (that is directed from divider 306 to phase detector 309 in Figure 3) that results from sigma delta modulator output signal 601. Figure 6b shows the divider output signal 604 that results from sigma delta modulator output signal 602.

A change in division, which occurs whenever the sigma delta modulator output signal changes its value (e.g., from 0 to +1 or +1 to 0), causes a slight change in the width of the pulses in the divider output signals 603, 604 (which are indistinguishable as drawn in Figure 6). The changes in pulse width subsequently cause the formation of one or more output pulses from phase detector 309. Thus, the frequency of the phase detector output signal is proportional to how often the sigma delta modulator output signal changes its value (i.e., the frequency of the sigma delta modulator output signal).

Figure 6a shows an exemplary phase detector output signal 605 that results from divider output signal 603 and Figure 6b shows an exemplary phase detector output signal 606 that results from divider output signal 604. Note that, for simplicity, only one output pulse is shown per change in division. Because sigma delta modulator signal 601 has three output value changes in time 650 while sigma delta modulator signal 602 has two output value changes in time 650, phase detector output signal 605 is a higher frequency signal than phase detector signal 606. That is, $T_{605}$ is less than $T_{606}$.

As a result, referring to Figures 3 and 6a,b, the lower frequencies associated with phase detector output signal 606 will be closer to the passband of loop filter 310 in Figure 3 than the higher frequencies associated with phase detector output signal 605. The lower frequencies associated with signal 606 are apt to be passed (rather than adequately filtered) by loop filter 311 causing the output voltage of loop filter 310 to have a time varying characteristic.

However, because signal 605 is a higher frequency signal than signal 606, the higher frequencies associated with signal 605 are apt to be adequately filtered (rather than passed) by loop filter 311 causing the output voltage of loop filter 311 to be approximately constant rather than time varying. The time

varying loop filter 311 output voltage associated with signal 606, in view of the absence of such variation from signal 605, causes the excessive jitter that is observed in the VCO output signal produced by sigma delta modulator signal 602 and that is not observed in the VCO output signal produced by sigma delta modulator output signal 601.

A solution to the sigma delta modulator output signal dependent jitter problem discussed above is presented in Figure 7. In Figure 7, a sigma delta modulator 702 output signal 710 is summed with a compensation signal 715. The compensation signal 715, which is produced by compensation circuit 716, is used to adjust the $SDO_{AVE}$ and/or increase the number of changes per unit of time in the sigma delta modulator output signal 710 before presentation to the input of the divider 706 that controls its division. Adjusting the sigma delta modulator output signal 710 in this manner results in the correct division for the channel being selected while keeping the jitter at the VCO output within an acceptable range.

According to this approach, for one or more channels the circuit if Figure 7 is designed to help demodulate, the sigma delta modulator output signal 710 is understood to be unsuitable for directly driving the divider as a result of : 1) its $SDO_{AVE}$ value and/or; 2) its frequency. The compensation signal 715 compensates for these deficiencies by: 1) adjusting the average value of the signal 710 (in the former case); and/or 2) adding more changes per unit of time to the signal 710 (in the later case).

A control word logic circuit 703 is used to translate an indication of the desired channel (presented at the channel select input 741) into a control word that is submitted to the sigma delta modulator 702. The channel select input 741 (or, alternatively, an output of the control word logic circuit 703) is used as an input to compensation circuit 716. The compensation circuit 716 produces a proper compensation signal 715 in light of the understood unsuitable nature of the sigma delta modulator output signal 710 for the channel being selected.

For example, recall from the discussion above concerning the embodiment of Figure 4 that excessive jitter may be observed when attempting to demodulate channel 20 because the sigma delta modulator output signal has a $SDO_{AVE}$ value that approaches an output value of the sigma delta modulator (which drops the frequency of the sigma delta modulator output signal). In one approach, in order to reduce jitter to within acceptable limits, the control word logic circuit 703 is configured to output a control word that will produce a sigma delta modulator output signal having: 1) an incorrect $SDO_{AVE}$ value for the channel to be received; but 2) a greater offset from a sigma delta modulator output value than the correct $SDO_{AVE}$ value for the selected channel (where an offset is the absolute value of the difference between an average value and a sigma delta modulator output value).

As a result, the sigma delta modulator output signal 710 with the incorrect $SDO_{AVE}$ value will have a greater frequency than the unused sigma delta modulator output signal having the correct $SDO_{AVE}$ value. The jitter at the VCO output signal is consequently reduced.

The compensation signal 715 produced by the compensation circuit 716 is then used to correct the $SDO_{AVE}$ value of the signal from the sigma delta modulator 702 before being presented to the divider 706 so that the proper channel (i.e., the channel corresponding to the channel select input 741) is received. Note that the indicia discussed above (with respect to Figures 5a and 5b) for comparing sigma delta modulator output signals may be used to understand whether the sigma delta modulator output signal having an incorrect $SDO_{AVE}$ value has a higher frequency than the sigma delta modulator signal having the correct $SDO_{AVE}$ value.

An example of such an approach is presented in Figure 8. The approach of Figure 8 compensates for the jitter associated with an exemplary design in which channel 27 is received with an $N_{AVE}$ of 93.000 and channel 1 received with an $N_{AVE}$ of 92.000. Note that for ease of illustration the receiver design of Figure 8 is different than the receiver design of Figure 4.

In Figure 8, region 850 corresponds to channels 1 through 27. Regions 851 and 852 correspond to regions that would normally have unacceptable jitter because of their proximity to a discrete output level of the sigma delta modulator as discussed above. Note that the exact boundaries of regions 851, 852 for any particular embodiment may be identified by a designer of ordinary skill in light of the tolerances associated with the designer's application.

In order to reduce the jitter in the VCO output, for channel select input values corresponding to region 851, the control word logic circuit 703 of Figure 7 may be configured to produce a control word that produces a sigma delta modulator output signal having an $SDO_{AVE}$ value within region 853 rather than region 851. For example, consider channel 1 within region 851. In the embodiment of Figure 8, a correct $SDO_{AVE}$ value for channel 1 is 0.000. However, according to the particular example shown in Figure 8, the control word logic circuit 703 is configured to present a control word for channel 1 that produces a sigma delta modulator output signal having an incorrect $SDO_{AVE}$ value of -0.500.

Note that the incorrect $SDO_{AVE}$ value (of –0.500) has an offset of 0.500 from either the 0 or –1 sigma delta modulator output values. An offset of 0.500 is greater than the offset associated with the correct $SDO_{AVE}$ value because, for channel 1, there is no offset between the correct $SDO_{AVE}$ value (0.000) and the sigma delta output value (0). Thus, although the $SDO_{AVE}$ value of the sigma delta modulator output signal is incorrect for direct demodulation of channel 1, the incorrect sigma delta modulator output signal is a higher frequency signal than the correct sigma delta modulator output signal.

Referring back to Figure 7, in order to receive the proper channel (i.e., the channel corresponding to the channel select input 741), the compensation signal 715 that is produced by the compensation circuit 716 is used to correct the $SDO_{AVE}$ value of the sigma delta modulator output signal 710 before presentation to the divider 706. In the embodiment of Figure 7, the compensation signal 715 is added to the sigma delta modulator output signal 710.

Straightforward mathematical derivation can be used to show that the average value of the signal 717 presented to the divider 706 (which may be expressed as $Correct_{AVE}$) is the summation of the average value of the compensation signal 715 (which may be expressed as $CS_{AVE}$) and the average value of the sigma delta modulator output signal 710 (which is expressed as $SDO_{AVE}$). That is:

$$Correct_{AVE} = CS_{AVE} + SDO_{AVE} \qquad \text{Eqn. 8.}$$

Referring briefly to Figure 8, for channel 1 as discussed in the example above, $Correct_{AVE} = 0.000$ and $SDO_{AVE} = -0.500$. Substitution into equation 8 yields, $CS_{AVE} = 0.500$. Thus, a compensation signal 715 having a $CS_{AVE}$ of 0.500 may be added to a sigma delta modulator output signal having an $SDO_{AVE} = -0.500$ in order to form an input signal 717 to the divider 706 having both the correct average value of 0.000 as well as a sufficient number of pulses to keep jitter at the VCO output within tolerable limits.

A suitable compensation signal 715 for this example is a clock signal. A clock signal may be represented by the repeating series +1, 0, +1, 0, etc. and therefore has an average value of 0.500. Note that many other signals having an average value of 0.500 besides clock signals are possible as well (e.g., as just one other example +2, -1, +2, -1, etc.). The clock signal may be the same signal (or a signal derived from the signal) used as the reference frequency signal that it is input to the phase detector within the phase lock loop circuit

Note that the divider 706 should be designed to handle each of the possible discrete levels produced by the summation of sigma delta modulator output signal 710 and the compensation signal 715. For example, the addition of a sigma delta modulator output signal having at least one output at each of the four output values –1, 0, +1, +2 to a clock signal representing a +1,0,+1,0, etc. repeating sequence will produce a signal having five output values of –1,0,+1,+2,+3. Thus, unlike the divider 306 design embodiment discussed with respect to Figure 3 (having four available division factors of N-1/N/N+1/N+2);

a divider 706 embodiment used for the present example should have five available division factors of N-1/N/N+1/N+2/N+3.

Referring back to Figure 8, each channel within region 851 may be demodulated with a sigma delta modulator output signal having an incorrect $SDO_{AVE}$ value that falls within region 853. Note that $CS_{AVE}$ may be a constant. That is, the difference between $Correct_{AVE}$ and $SDO_{AVE}$ may be the same for each channel within region 851. If $CS_{AVE}$ is constant, then the same compensation signal may be used for each channel. That is, if each incorrect $SDO_{AVE}$ value has an error of –0.500, a signal having an average value of +0.500 (e.g., a clock signal) may be used to compensate each channel.

Referring 9 shows an example of a circuit that conforms to the approach shown in Figure 7. The compensation circuit 916 of Figure 9, contains a multiplexer 930 having an enable input 931 coupled to decode logic 932. Decode logic 932 is designed to identify whether a compensation signal is needed or not needed.

Referring to Figures 8 and 9, recall that of the channels within sub band 850 only channels within regions 851 and 852 exhibit unacceptable jitter if demodulated directly with an uncompensated sigma delta modulator output signal having $SDO_{AVE} = Correct_{AVE}$. The channels within region 855, therefore, may be demodulated directly by a sigma delta modulator output signal having the correct $SDO_{AVE}$ value for the channel being selected. Thus, if the channel select input 941 corresponds to a channel that can be adequately demodulated when $SDO_{AVE} = Correct_{AVE}$, the control word logic circuit 903 is configured to present a control word to the sigma delta modulator 902 that will produce a sigma delta modulator output signal having the correct $SDO_{AVE}$ value.

Furthermore, in this case a compensation signal is not needed. Thus, the decode logic 932 is configured to present an enable input value to the multiplexer 932 that corresponds to input B of the multiplexer 930. As seen in Figure 9, there is no effective signal (i.e., a null signal) at the input B of the multiplexer 930. That is, adding 0 to the sigma delta modulator output signal

will not adjust the sigma delta modulator output signal in any way. This results in the presentation to the divider 906 of the pure sigma delta modulator 902 output signal.

If the channel select input 941 corresponds to a channel that would exhibit unacceptable jitter if demodulated with an uncompensated sigma delta modulator output signal having $SDO_{AVE} = Correct_{AVE}$ (such as a channel within regions 851 or 853 in the example of Figure 8), the decode logic 932 is configured to present an input enable value to the multiplexer 932 that corresponds to input A of the multiplexer 930.

As seen in Figure 9, the compensation signal is used as the input to A of the multiplexer 930. If a clock is used for the compensation signal, the adder 970 may be configured to interpret the clock signal as a signal exhibiting a +1,0,+1,0, etc. sequence. As such, the $SDO_{AVE}$ value of the sigma delta modulator output signal will be increased by 0.500 before presentation to the divider 906.

Furthermore, in this case, the control word logic circuit 903 should be configured to present a control word to the sigma delta modulator 902 that will produce a sigma delta modulator output signal having an incorrect value of $SDO_{AVE} = Correct_{AVE} - CS_{AVE}$. Thus, if the compensation signal is the same clock signal described above, an $SDO_{AVE}$ value that is 0.500 less than the $Correct_{AVE}$ value for the channel being selected should be used.

The control word logic circuit 903 may be implemented with a look-up table or with logic. If the control word logic circuit 903 is implemented as a look up table, a listing of the channel select input 941 and the corresponding control word may be stored within the lookup table for each channel. Thus, using the approach of Figure 8 as an example, if a particular channel select input 941 value corresponding to region 855 is presented, the control word logic circuit 903 outputs a control word having the correct $SDO_{AVE}$ value for the particular channel.

Also, when a particular channel select input 941 value corresponding to regions 851 or 852 is presented, the control word logic circuit 903 outputs a

control word having the incorrect $SDO_{AVE}$ value for the particular channel. Those of ordinary skill can determine the control word needed to produce a sigma delta modulator output signal having a desired $SDO_{AVE}$ value, whether "correct" or "incorrect" as discussed above.

The decode logic 932 may also be implemented with a look-up table or with logic. If the decode logic 932 is implemented with a look up table, a listing of the channel select input 941 and the proper input enable value may be stored for each channel. Thus, for example, when a channel select input value corresponding to region 855 is presented, the decode logic 932 outputs an input enable value that corresponds to input B of the multiplexer; and, when a channel select input value corresponding to regions 851 or 852 is presented, the decode logic 932 outputs an enable input value that corresponds to input A of the multiplexer.

Note that in an alternative embodiment, the decode logic 932 can be merged with the control word logic circuit 903 rather than be implemented within the compensation circuit 916. In such an embodiment, the control word logic circuit has two outputs, one directed to the sigma delta modulator 902 and another directed to the compensation circuit 916. The output directed to the sigma delta modulator 902 presents the sigma delta modulator with the control word for the channel to be demodulated; and the output directed to the multiplexer 930 provides enable input information.

In another alternative embodiment, the decode logic 932 is located within the compensation circuit 916 but is also configured to determine the proper channel select value based upon the control word from the control word logic circuit 903 rather than the channel select input 941. In both of the alternate embodiments discussed above, the channel select input 941 does not need to be coupled to the compensation circuit 916.

Note that the circuits of Figures 7 and 9 may continue to be used when more than one region within the band or sub band of interest exhibits unacceptable jitter with an uncompensated sigma delta modulator output signal

having an $SDO_{AVE} = Correct_{AVE}$. As an example, an explanation of how the embodiment of Figure 9 may be configured to properly demodulate the channels within region 852 of Figure 8 immediately follows.

Continuing with the example where the compensation signal corresponds to a clock signal, recall that the clock signal adds 0.500 to the $SDO_{AVE}$ value of the sigma delta modulator output signal. Thus, consistent with equation 8, $CS_{AVE}$ = 0.500 and $SDO_{AVE}$ should be set equal to $Correct_{AVE} - 0.500$. If the channel select input 941 corresponds to a channel within region 852, the control word logic circuit 903 should be configured to present the sigma delta modulator 902 with a control word that produces a sigma delta modulator output signal having an $SDO_{AVE}$ value that is 0.500 less than the $Correct_{AVE}$ for the channel being selected.

Note that the control word may correspond to a control word used to demodulate a signal within region 855. However, because the decode logic 932 should also be configured to select channel A of the multiplexer 930 for a channel select input 941 within region 852, the "incorrect" $SDO_{AVE}$ associated with the sigma delta modulator output signal is corrected for and the proper channel within region 852 is demodulated rather than a channel within region 855.

It is important to note that compensation signals other than a clock signal interpreted as a +1,0,+1, 0 sequence may be used. Designers may configure the adjustment performed by the compensation signal by considering the polarity, amplitude, offset, duty cycle and frequency of the compensation signal. Recall that the average value of the compensation signal $CS_{AVE}$ corresponds to the adjustment made by the compensation signal to the $SDO_{AVE}$ of the sigma delta modulator output signal. Thus, because the average value of a signal is determined by its polarity, amplitude, offset, duty cycle and frequency; the precise adjustment made by the compensation signal to the sigma delta modulator output signal may be determined in light of these signal properties.

Polarity may be affected by performing (or not performing) inversion. For example, if an inverter is inserted between a clock source and the input to

channel A of the multiplexer 930 of Figure 9, a +1,0,+1,0, etc. clock signal having an average value of 0.500 will be converted into a –1,0,-1,0,etc. compensation signal having an average value of –0.500. Amplitude may be determined by controlling the output levels of the compensation signal (e.g.,, by an amplifier or otherwise). For example, a +1,0,+1,0, etc. clock signal having an average value of 0.500 can be converted by a 2x amplifier into a +2,0,+2,0, etc. compensation signal having an average value of 1.000.

Offset may be affected by controlling the level of the compensation signal. For example, a +1,0,+1,0, etc. clock signal having a 0.500 average value can be converted by a -1 level shifter into a 0,-1,0,-1, etc. compensation signal having a –0.500 average value. Duty cycle may be determined by controlling the number of pulses per repetition period of the compensation signal and/or the time width of the pulses themselves. Note that if two signals have equal duty cycle but different frequency, the two signals will have a different average value. Likewise, if two signals have the same frequency but different duty cycle, the two signals will have a different average value.

Frequency may be determined by dividing a clock signal (e.g., via a divider) or multiplying (e.g., via a clock multiplier) a clock signal. Caution should be exercised when the frequency of the compensation signal is being determined. On the low end, the frequency of the compensation signal should be high enough such that jitter does not appear at the VCO output (i.e., sufficiently above the passband of the loop filter).

On the high end, the frequency of the compensation signal should be within the bandwidth of both the divider and the phase comparator so that both can properly process the signals presented to them. Note that the frequency of the compensation signal can be equal to or can be derived from the clock source that clocks the sigma delta modulator and/or operates as the local oscillator input to the phase comparator. In some cases this may be a requirement (e.g., if the divider 906 is a synchronous device that only recognizes value changes from the adder 950 of Figure 9 at intervals timed according to the local oscillator).

In one embodiment, the average value $CS_{AVE}$ of the compensation signal may be 0 if the frequency of the compensation signal is enough to remove the jitter at the VCO output. For example, the compensation may be used to add more changes per unit of time to the sigma delta modulator output signal rather than adjust its $SDO_{AVE}$ value. An example of such a compensation signal is a signal that is balanced above and below the 0 level (e.g., a sequence that repeats according to +1, -1, +1, -1, etc.). Note that, in light of Equation 8, if $CS_{AVE} = 0$ then $SDO_{AVE} = Correct_{AVE}$. That is, the sigma delta modulator output signal does not require an incorrect $SDO_{AVE}$ value.

As such, the control word logic circuit 703 need only present to the sigma delta modulator control words that correspond to the correct channel (e.g., in the example of Figure 8, only control words within region 850 are presented) even if a channel exhibits unacceptable jitter. The frequency of the compensation signal that may be used for such an approach will depend upon the bandwidth of the loop filter. Generally, as the frequency of the compensation signal extends beyond the passband of the loop filter, this embodiment may be utilized. Note that in typical embodiments the clock source fed to the phase detector typically exceeds the pass band of the loop filter.

For whatever compensation signal that the designer decides is best for his or her application, other than a pure clock signal as seen in Figure 9, the offset, amplitude, duty cycle, and/or frequency may be tailored within the compensation circuits 716, 916 of Figures 7 and 9. For example, referring to Figure 9, compensation signal shaping circuitry that affects the polarity, amplitude, offset, duty cycle and/or frequency may be inserted between a clock source and the input to channel A of the multiplexer 930.

Some embodiments may also effectively tailor (partially or completely) the compensation signal by adding signal shaping functionality into the adder 950 or between the multiplexor 930 output and the adder 950. For example, by inserting an inverter in front of the input to the adder 950 of Figure 9, the compensation signal will adjust the $SDO_{AVE}$ of the sigma delta modulator output

signal by –0.500 rather than 0.500. Note that in some cases, compensation signal shaping circuitry inserted in the adder or between the adder and multiplexor 930 output will affect the proper "null" signal at channel B of the multiplexer 930. For example, if a –1.000 level shifter is inserted just before the input to the adder 950, a +1 null signal should be presented to the channel B input rather than a "0" input.

Note that the techniques discussed herein extend to various ways in which the compensation signal and sigma delta modulator output signal may be combined rather than just added. Thus, more generally, the adder 750, 950 of Figures 7 and 9 may be replaced by a combination unit that adds, subtracts or otherwise combines the compensation signal and sigma delta modulator output signal together to produce a signal ultimately used to control the division performed by the divider 706, 906.

In still other embodiments, additional functionality may be inserted between the signal from the combination unit 750, 950 and the divider. For example, the signal from the combination unit 750, 950 may be adjusted as to its polarity, offset, amplitude, duty cycle or frequency before presentation to the divider.

Logic or other functionality devoted to this purpose may be referred to as "post combination" circuitry because it processes the signal that results from the combination of the compensation signal and the sigma delta modulator output signal. Regardless if post combination circuitry exists or not, the output of the combination unit 750, 950 may be said to control the division performed by the divider 706, 906.

In still other embodiments, the additional functionality may be inserted between the sigma delta modulator 702, 902 and the combination unit. For example, the signal from the sigma delta modulator 702, 902 may be adjusted as to its polarity, offset, amplitude, duty cycle or frequency before presentation to the combination unit 750, 950. If such functionality exists it may be viewed as an output stage of the sigma delta modulator 702, 902.

Again, note that in many of the examples above the compensation signal has an absolute value of 0.500. It is important to point out that this has been done for illustrative convenience. In practice a designer may choose any average value that is appropriate for the application (e.g., 0.000, 0.100, 0.200, 0.250, 0.300, are just a few of a number of possibilities). Regardless of the average value of the compensation signal, however, the $SDO_{AVE}$ value associated with the sigma delta modulator output signal should be consistent with equation 8 provided above.

Furthermore, for any compensation signal, note that the divider should be configured to accept each level that the combination of the sigma delta modulator output signal and the compensation signal will produce. For example, when added together, a sigma delta modulator output signal having four levels of –1/0/+1/+2 and a compensation signal that is a repeating +2,0,+2,0, etc., sequence will produce a signal for presentation to the divider having levels of –1/0/+1/+2/+3/+4 if each sigma delta modulator output level is added to both levels (0,+2) of the compensation signal.

Figure 10 summarizes the operation of the circuits shown in Figures 7 and 9. After presentation of a channel select value, the circuit (e.g., via entries in a look up table) presents 1101 a control word to a sigma delta modulator. If a compensation signal is needed, a compensation signal is combined 1003 (e.g., via addition or subtraction) with a sigma delta modulator output signal before being forwarded 1004 to a divider. If a compensation signal is not needed, a sigma delta modulator output signal is forwarded 1005 to a divider.

Note that the use of average value examples to three or four decimal places has been done for convenience. Practical applications may require resolution of $SDO_{AVE}$, $CS_{AVE}$, and $Correct_{AVE}$ beyond three decimal places.

Discussion of Signal Frequency Indicia

The following discussion, which refers to Figure 5, is an elaboration of signal frequency indicia mentioned above. Note that both output signals 501, 502 are repeating patterns. The pattern that repeats for signal 501 is shown within time period 507 while the pattern that repeats for signal 502 is shown within time period 506. Careful analysis indicates that within time period 507, signal 501 has 105 pulses above or below its corresponding $SDO_{AVE}$ value of 0.500; and, within time period 507, signal 502 has 19 pulses above or below its corresponding $SDO_{AVE}$ value of 1.000.

Because time period 507 is a factor of 4.088 longer than time period 506, signal 501 exhibits 25.6 pulses per unit of time while signal 502 has 19.0 pulses per unit of time (i.e., 105/4.088 = 25.6; 19/1 = 19.0). Because each pulse observed in signals 501, 502 corresponds to a change in the value of the output signal, signal 501 exhibits more changes per unit of time than signal 502.

Also, as seen by comparing signal 501 with signal 502, note that signal 501 exhibits a lesser percentage of consecutive, equal output values than signal 502. A detailed analysis indicates that the repeating pattern of signal 501 has 139 separate values within time period 507. Of these 139 separate values, 36 are neighboring an identical output value. That is, regions a through r correspond to 18 regions having either two consecutive output values of +1 or two consecutive output values of 0 (i.e., a sequence of +1, +1 or a sequence of 0,0). Eighteen regions of two consecutive output values correspond to 36 output values having an identically valued neighbor. As 36 out of 139 output values have an identically valued neighbor, 25.9% of signal 501 has consecutive, equal output values.

A similar analysis indicates that the repeating pattern of signal 502 has 34 separate values within time period 506. Of these 34 separate values, 10 are neighboring an identical output value. That is, regions s and t of signal 502 corresponds to three consecutive output values of +1 (i.e., a sequence of +1, +1, +1); while regions u and v correspond to two consecutive output values of +1 (i.e., a sequence of +1, +1). Two regions of three consecutive, equal output

values and two regions of two, equal output values correspond to 10 output values having an identically valued neighbor (i.e., (3x2)+(2x2)=6+4=10). As 10 out of 34 output values have an identically valued neighbor, 29.4% of signal 502 has consecutive, equal output values.

If a first signal (such as signal 501) has a smaller percentage of consecutive, equal output values than a second signal (such as signal 502), the first signal will correspondingly have more changes per unit of time than the second signal. That is, the first signal is a higher frequency signal than the second signal. Thus, the analysis just presented above corresponds to another way in which the frequency associated with a pair of sigma delta modulator output signals may be compared.

Furthermore, note that signal 502 tends to use more output values when transitioning from a relative minimum value to a relative maximum value. A relative minimum occurs whenever the middle value of three different output values is lower than the other two output values. For example output value 531 of signal 501, having a value of –1, is a relative minimum because the previous different output value 530 is +2 and the following output value 532 is +2.

A relative maximum occurs whenever the middle value of three different output values is greater than the other two output values. For example output value 532 of signal 501, having a value of +2, is a relative maximum because the previous different output value 531 is –1 and the following output value 533 is –1. Note that in the transition from relative minimum 531 to relative maximum 532, there are no intervening output values. That is, the output signal 501 swings directly from relative minimum 531 to relative maximum 532 within one resolution period.

Comparing this behavior with the behavior of signal 502, note the existence of an intervening output value during the transition from relative minimum 534 to relative maximum 535. That is, the transition from relative minimum 534 to relative maximum 535 occurs via a sequence of –1,+1,+2 which consumes two resolution periods. As the transition from –1 to +2 associated

with signal 501 occurs within one resolution period whereas the transition from –1 to +2 associated with signal 502 occurs within two resolution periods, the transition associated with signal 501 is more abrupt than the transition associated with signal 502.

Careful comparison of signal 501 with signal 502 will indicate that: 1) signal 501 has more transitions from a relative minimum to a relative maximum that occur within a single resolution period; 2) signal 501 has more transitions from a relative maximum to a relative minimum that occur within a single resolution period; 3) signal 501has less intervening output values, on average, per transition from a relative minimum to a relative maximum; and 4) signal 501 has less intervening output values, on average, per transition from a relative maximum to a relative minimum. The above are all indicia that signal 501 exhibits more abrupt change in output signal value per unit of time than signal 502 and therefore may be viewed as a higher frequency signal.

It is important to point out that the discussion above is applicable to other applications besides operation within a BLUETOOTH device. The teachings above may be applied to any design that employs Fractional N synthesis jitter. Thus, for example, the present teachings are also applicable to other wireless technologies besides besides BLUETOOTH such, as just a few examples, HomeRF, IEEE 802.11, GSM and Digitally Enhanced Cordless Telephony (DECT).

Embodiments of the discussion may be manufactured as part of a semiconductor chip (e.g., by being manufactured with a planar semiconductor manufacturing process). Note also that embodiments of the present description may be implemented not only as part of a semiconductor chip but also within machine readable media. For example, the designs discussed above may be stored upon and/or embedded within machine readable media associated with a design tool used for designing semiconductor devices. Examples include a netlist formatted in the VHSIC Hardware Description Language (VHDL) language, Verilog language or SPICE language. Some netlist examples include:

a behaviorial level netlist, a register transfer level (RTL) netlist, a gate level netlist and a transistor level netlist. Machine readable media also include media having layout information such as a GDS-II file. Furthermore, netlist files or other machine readable media for semiconductor chip design may be used in a simulation environment to perform the methods of the teachings described above.

Thus, it is also to be understood that embodiments of this invention may be used as or to support a software program executed upon some form of processing core (such as the CPU of a computer) or otherwise implemented or realized upon or within a machine readable medium. A machine readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine readable medium includes read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; electrical, optical, acoustical or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.); etc.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

## CLAIMS

What is claimed is:

1. A method, comprising:
combining a sigma delta modulator output signal with a second signal to form a third signal that controls the division performed by a divider.

2. The method of claim 1 wherein said division performed by said divider controls the frequency multiplication performed by a phase lock loop circuit.

3. The method of claim 2 wherein said frequency multiplication performed by said phase lock loop circuit produces a fourth signal having a frequency used to receive information within a desired channel.

4. The method of claim 3 wherein a fifth signal received from an antennae is multiplied by said fourth signal or multiplied by a sixth signal generated from said fourth signal.

5. The method of claim 2 wherein said frequency multiplication performed by said phase lock loop circuit produces a fourth signal having a frequency used to transmit information within a desired channel.

6. The method of claim 1 wherein said second signal is a clock signal.

7. The method of claim 1 wherein said combining further comprises adding said sigma delta modulator output signal to said second signal.

8. The method of claim 1 further comprising presenting a control word to a sigma delta modulator in order to produce said sigma delta modulator output signal.

9. The method of claim 8 wherein the value of said control word is determined by which of a plurality of channels is to be selected.

10. The method of claim 1 wherein said second signal is nullified if said sigma delta modulator output signal has a correct average value for receiving or transmitting information within a desired channel.

11. The method of claim 1 wherein said sigma delta modulator output signal is unsuitable for controlling said division so as to receive or transmit information within a desired channel, said third signal compensating for said unsuitability.

12. The method of claim 11 wherein said unsuitability is an incorrect average value, said third signal having an average value equal to the difference between said correct average value and said incorrect average value, said third signal having said correct average value.

13. A method, comprising:

a) generating a sigma delta modulator output signal having an incorrect average value for a desired channel, a correct average value for said desired channel having a first offset from a nearest output value of said sigma delta modulator, said incorrect average value having a second offset from said nearest output value of said sigma delta modulator, said first offset less than said second offset, and

b) combining said sigma delta modulator output signal with a compensation signal, said compensation signal having an average value that compensates for said incorrect average value so that a signal having said correct average value for said desired channel is produced.

14. The method of claim 13 wherein said second offset is 0.5.

15. The method of claim 14 wherein said compensation signal is a reference frequency signal that is presented to the input of a phase detector within a phase lock loop circuit.

16. The method of claim 13 wherein said second offset is the same for at least one other desired channel.

17. The method of claim 13 wherein said incorrect average value corresponds to a band region or sub band region used for other channels.

18. The method of claim 17 wherein said incorrect average value is a correct average value for another channel.

19. The method of claim 13 wherein said incorrect average value is less than said correct average value.

20. The method of claim 13 further comprising controlling the division performed by a divider with said signal.

21. The method of claim 20 wherein said division is N + $Correct_{AVE}$ where N is the division of said divider when said signal has a value of 0.0 and $Correct_{AVE}$ is said correct average value.

22. The method of claim 20 wherein said division performed by said divider further comprises performing a different division for each discrete value of said signal.

23. The method of claim 20 wherein said division performed by said divider controls the frequency multiplication performed by a phase lock loop circuit.

24. The method of claim 23 wherein said frequency multiplication performed by said phase lock loop circuit produces a second signal having a frequency used to receive information within said desired channel.

25. The method of claim 24 wherein a third signal received from an antennae is multiplied by said second signal or multiplied by a fourth signal generated from said second signal.

26. The method of claim 23 wherein said frequency multiplication performed by said phase lock loop circuit produces a fourth signal having a frequency used to transmit information within a desired channel.

27. The method of claim 13 wherein said combining further comprises adding said sigma delta modulator output signal to said compensation signal.

28. The method of claim 13 further comprising presenting a control word to said sigma delta modulator.

29. The method of claim 28 further comprising looking up said control word based upon said desired channel.

30. The method of claim 13 further comprising changing the polarity of a clock signal or changing the polarity of a second signal that is derived from a clock signal to help form said compensation signal.

31. The method of claim 30 wherein said clock signal is also presented to the input of a phase detector within a phase lock loop circuit.

32. The method of claim 13 further comprising changing a clock signal offset or changing the a second signal offset, said second signal derived from a clock signal to help form said compensation signal.

33. The method of claim 32 wherein said clock signal is also presented to the input of a phase detector within a phase lock loop circuit.

34. The method of claim 13 further comprising changing the amplitude of a clock signal or changing the amplitude of a second signal that is derived from a clock signal to help form said compensation signal.

35. The method of claim 34 wherein said clock signal is also presented to the input of a phase detector within a phase lock loop circuit.

36. The method of claim 13 further comprising changing the duty cycle of a clock signal or changing the duty cycle of a second signal that is derived from a clock signal to help form said compensation signal.

37. The method of claim 36 wherein said clock signal is also presented to the input of a phase detector within a phase lock loop circuit.

38. The method of claim 13 further comprising changing the frequency of a clock signal or changing the frequency of a second signal that is derived from a clock signal to help form said compensation signal.

39. The method of claim 38 wherein said clock signal is also presented to the input of a phase detector within a phase lock loop circuit.

40. A method, comprising:

a) generating a sigma delta modulator output signal having an incorrect average value for a desired channel, said sigma delta modulator output signal having a greater frequency than a sigma delta modulator output signal having a correct average value for said desired channel; and

b) combining said sigma delta modulator output signal having said incorrect average value with a compensation signal, said compensation signal having an average value that compensates for said incorrect average value so that a signal having said correct average value for said desired channel is produced.

41. The method of claim 40 wherein said sigma delta modulator output signal having said incorrect average value has more changes per unit of time than said sigma delta modulator output signal having said correct average value.

42. The method of claim 41 wherein said sigma delta modulator output signal having said incorrect average value has more pulses per unit of time than said sigma delta modulator output signal having said correct average value.

43. The method of claim 41 wherein said sigma delta modulator output signal having said incorrect average value has less consecutive, equal output values per unit of time than said sigma delta modulator output signal having said correct average value.

44. The method of claim 40 wherein said sigma delta modulator output signal having said incorrect average value has more transitions from a relative minimum to a relative maximum that occur within a single resolution period than said sigma delta modulator output signal having said correct average value.

45. The method of claim 40 wherein said sigma delta modulator output signal having said incorrect average value has more transitions from a relative maximum to a relative minimum that occur within a single resolution period than said sigma delta modulator output signal having said correct average value.

46. The method of claim 40 wherein said sigma delta modulator output signal having said incorrect average value has less intervening output values, on average, per transition from a relative minimum to a relative maximum than said sigma delta modulator output signal having said correct average value.

47. The method of claim 40 wherein said sigma delta modulator output signal having said incorrect average value has less intervening output values, on average, per transition from a relative maximum to a relative minimum than said sigma delta modulator output signal having said correct average value.

48. The method of claim 40 wherein said incorrect average value corresponds to a band region or sub band region used for other channels.

49. The method of claim 48 wherein said incorrect average value is a correct average value for another channel.

50. The method of claim 40 wherein said incorrect average value is less than said correct average value.

51. The method of claim 40 further comprising controlling the division performed by a divider with said signal.

52. The method of claim 51 wherein said division is N + $Correct_{AVE}$ where N is the division of said divider when said signal has a value of 0.0 and $Correct_{AVE}$ is said correct average value.

53. The method of claim 51 wherein said division performed by said divider further comprises performing a different division for each discrete value of said signal.

54. The method of claim 51 wherein said division performed by said divider controls the frequency multiplication performed by a phase lock loop circuit.

55. The method of claim 54 wherein said frequency multiplication performed by said phase lock loop circuit produces a second signal having a frequency used to receive information within said desired channel.

56. The method of claim 55 wherein a third signal received from an antennae is multiplied by said second signal or multiplied by a fourth signal generated from said second signal.

57. The method of claim 54 wherein said frequency multiplication performed by said phase lock loop circuit produces a fourth signal having a frequency used to transmit information within a desired channel.

58. The method of claim 40 wherein said combining further comprises adding said sigma delta modulator output signal to said compensation signal.

59. The method of claim 40 further comprising presenting a control word to said sigma delta modulator.

60. The method of claim 59 further comprising looking up said control word based upon said desired channel.

61. The method of claim 40 wherein said compensation signal is a clock signal.

62. The method of claim 61 wherein said clock signal is also presented to the input of a phase detector within a phase lock loop circuit.

63. The method of claim 40 further comprising changing the polarity of a clock signal or changing the polarity of a second signal that is derived from a clock signal to help form said compensation signal

64. The method of claim 63 wherein said clock signal is also presented to the input of a phase detector within a phase lock loop circuit.

65. The method of claim 40 further comprising changing the offset of a clock signal or changing the offset of a second signal that is derived from a clock signal to help form said compensation signal.

66. The method of claim 65 wherein said clock signal is also presented to the input of a phase detector within a phase lock loop circuit.

67. The method of claim 40 further comprising changing the amplitude of a clock signal or changing the amplitude of a second signal that is derived from a clock signal to help form said compensation signal.

68. The method of claim 67 wherein said clock signal is also presented to the input of a phase detector within a phase lock loop circuit.

69. The method of claim 40 further comprising changing the duty cycle of a clock signal or changing the duty cycle of a second signal that is derived from a clock signal to help form said compensation signal.

70. The method of claim 69 wherein said clock signal is also presented to the input of a phase detector within a phase lock loop circuit.

71. The method of claim 40 further comprising changing the frequency of a clock signal or changing the frequency of a second signal that is derived from a clock signal to help form said compensation signal.

72. The method of claim 71 wherein said clock signal is also presented to the input of a phase detector within a phase lock loop circuit.

73. A method, comprising:

a) presenting an input to a sigma delta modulator that produces a sigma delta modulator output signal having a correct average value for a desired channel; and

b) combining said sigma delta modulator output signal with a compensation signal to produce a signal, said compensation signal having a higher frequency than said sigma delta modulator output signal, said signal having said correct average value for said desired channel and a higher frequency than said sigma delta modulator output signal.

74. The method of claim 73 wherein said compensation signal has more changes per unit of time than said sigma delta modulator output signal having said correct average value.

75. The method of claim 74 wherein said compensation signal has more pulses per unit of time than said sigma delta modulator output signal having said correct average value.

76. The method of claim 74 wherein said compensation signal has less consecutive, equal output values per unit of time than said sigma delta modulator output signal having said correct average value.

77. The method of claim 73 wherein said compensation signal has more transitions from a relative minimum to a relative maximum that occur within a single resolution period than said sigma delta modulator output signal having said correct average value.

78. The method of claim 73 wherein said compensation signal has more transitions from a relative maximum to a relative minimum that occur within a single resolution period than said sigma delta modulator output signal having said correct average value.

79. The method of claim 73 wherein said compensation signal has less intervening output values, on average, per transition from a relative minimum to a relative maximum than said sigma delta modulator output signal having said correct average value.

80. The method of claim 73 wherein said compensation signal has less intervening output values, on average, per transition from a relative maximum to a relative minimum than said sigma delta modulator output signal having said correct average value.

81. An apparatus, comprising:

a) a sigma delta modulator that presents an output signal having an incorrect average value for a desired channel, a correct average value for said desired channel having a first offset from a nearest output value of said sigma delta modulator, said incorrect average value having a second offset from said nearest output value of said sigma delta modulator, said first offset less than said second offset; and

b) a combination unit having a first input for receiving said sigma delta modulator output signal, said combination unit having a second input for receiving a compensation signal , said compensation signal having an average

value that compensates for said incorrect average value so that a signal having said correct average value for said desired channel can be produced.

82. The apparatus of claim 81 wherein said second offset is 0.5.

83. The apparatus of claim 82 further comprising a phase comparator within a phase lock loop circuit having a reference frequency signal input, said reference frequency signal used as said compensation signal.

84. The apparatus of claim 81 wherein said second offset is the same for at least one other desired channel.

85. The apparatus of claim 81 wherein said incorrect average value corresponds to a band region or sub band region used for other channels.

86. The apparatus of claim 85 wherein said incorrect average value is a correct average value for another channel.

87. The apparatus of claim 81 wherein said incorrect average value is less than said correct average value.

88. The apparatus of claim 81 further comprising a divider having a divider input that controls the division performed by said divider, said divider input configured to receive said signal.

89. The apparatus of claim 88 wherein said division is $N + Correct_{AVE}$ where N is the division of said divider when said signal has a value of 0.0 and $Correct_{AVE}$ is said correct average value.

90. The apparatus of claim 88 wherein said divider has a different division factor for each discrete value of said signal.

91. The apparatus of claim 88 further comprising a phase lock loop circuit, said divider located within a feedback path of said phase lock loop circuit so that

said division controls a frequency multiplication performed by said phase lock loop circuit.

92. The apparatus of claim 91 further comprising a voltage controlled oscillator within said phase lock loop circuit, said voltage controlled oscillator output signal used to receive information within said desired channel, said voltage controlled oscillator output signal having a frequency determined by said frequency multiplication.

93. The apparatus of claim 92 further comprising a mixer coupled to an antennae and said voltage controlled oscillator.

94. The apparatus of claim 91 further comprising a voltage controlled oscillator within said phase lock loop circuit, said voltage controlled oscillator output signal used to receive information within said desired channel, said voltage controlled oscillator output signal having a frequency determined by said frequency multiplication.

95. The apparatus of claim 81 wherein said combination unit further comprises an adder.

96. The apparatus of claim 81 further comprising a control word logic circuit coupled to an input of said sigma delta modulator.

97. The apparatus of claim 96 further comprising a channel select input coupled to said control word logic circuit.

98. The apparatus of claim 81 further comprising a compensation circuit that at least partially forms said compensation signal, said compensation circuit having an output coupled to said second combination unit input.

99. The apparatus of claim 98 wherein said compensation circuit further comprises a multiplexer, said multiplexer having a multiplexer output coupled to said second input of said combination unit, a first multiplexer input that

receives said compensation signal, a second multiplexer input that receives a null signal and an input enable coupled to a decode logic output.

100. The apparatus of claim 81 further comprising a level shifter between a clock signal and said second input of said combination unit.

101. The apparatus of claim 100 wherein said clock signal is coupled to the input of a phase detector within a phase lock loop circuit.

102. The apparatus of claim 81 further comprising an amplifier between a clock signal and said second input of said combination unit.

103. The apparatus of claim 102 wherein said clock signal is also coupled to the input of a phase detector within a phase lock loop circuit.

104. The apparatus of claim 81 further comprising a duty cycle circuit between a clock signal and said second input of said combination unit.

105. The apparatus of claim 104 wherein said clock signal is also coupled to the input of a phase detector within a phase lock loop circuit.

106. The apparatus of claim 81 further comprising a circuit that changes frequency of clock signal, said circuit between said clock signal and said second input of said combination unit.

107. The apparatus of claim 106 wherein said clock signal is also presented to the input of a phase detector within a phase lock loop circuit.

108. An apparatus, comprising:

a) a sigma delta modulator that presents an output signal having an incorrect average value for a desired channel, said sigma delta modulator output signal having a greater frequency than a sigma delta modulator output signal having a correct average value for said desired channel; and

b) a combination unit having a first input for receiving said sigma delta modulator output signal having said incorrect average value, said combination unit having a second input for receiving a compensation signal , said compensation signal having an average value that compensates for said incorrect average value so that a signal having said correct average value for said desired channel can be produced.

109. The apparatus of claim 108 wherein said sigma delta modulator output signal having said incorrect average value has more changes per unit of time than said sigma delta modulator output signal having said correct average value.

110. The apparatus of claim 109 wherein said sigma delta modulator output signal having said incorrect average value has more pulses per unit of time than said sigma delta modulator output signal having said correct average value.

111. The apparatus of claim 109 wherein said sigma delta modulator output signal having said incorrect average value has less consecutive, equal output values per unit of time than said sigma delta modulator output signal having said correct average value.

112. The apparatus of claim 108 wherein said sigma delta modulator output signal having said incorrect average value has more transitions from a relative minimum to a relative maximum that occur within a single resolution period than said sigma delta modulator output signal having said correct average value.

113. The apparatus of claim 108 wherein said sigma delta modulator output signal having said incorrect average value has more transitions from a relative maximum to a relative minimum that occur within a single resolution period than said sigma delta modulator output signal having said correct average value.

114. The apparatus of claim 108 wherein said sigma delta modulator output signal having said incorrect average value has less intervening output values, on average, per transition from a relative minimum to a relative maximum than said sigma delta modulator output signal having said correct average value.

115. The apparatus of claim 108 wherein said sigma delta modulator output signal having said incorrect average value has less intervening output values, on average, per transition from a relative maximum to a relative minimum than said sigma delta modulator output signal having said correct average value.

116. The apparatus of claim 108 wherein said incorrect average value corresponds to a band region or sub band region used for other channels.

117. The apparatus of claim 116 wherein said incorrect average value is a correct average value for another channel.

118. The apparatus of claim 108 wherein said incorrect average value is less than said correct average value.

119. The apparatus of claim 108 further comprising a divider having a divider input that controls the division performed by said divider, said divider input configured to receive said signal.

120. The apparatus of claim 119 wherein said division is $N + Correct_{AVE}$ where N is the division of said divider when said signal has a value of 0.0 and $Correct_{AVE}$ is said correct average value.

121. The apparatus of claim 119 wherein said divider has a different division factor for each discrete value of said signal.

122. The apparatus of claim 119 further comprising a phase lock loop circuit, said divider located within a feedback path of said phase lock loop circuit so that

said division controls a frequency multiplication performed by said phase lock loop circuit.

123. The apparatus of claim 122 further comprising a voltage controlled oscillator within said phase lock loop circuit, said voltage controlled oscillator output signal used to receive information within said desired channel, said voltage controlled oscillator output signal having a frequency determined by said frequency multiplication.

124. The apparatus of claim 123 further comprising a mixer coupled to an antennae and said voltage controlled oscillator.

125. The apparatus of claim 123 further comprising a voltage controlled oscillator within said phase lock loop circuit, said voltage controlled oscillator output signal used to receive information within said desired channel, said voltage controlled oscillator output signal having a frequency determined by said frequency multiplication.

126. The apparatus of claim 108 wherein said combination unit further comprises an adder.

127. The apparatus of claim 108 further comprising a control word logic circuit coupled to an input of said sigma delta modulator.

128. The apparatus of claim 127 further comprising a channel select input coupled to said control word logic circuit.

129. The apparatus of claim 108 further comprising a compensation circuit that at least partially forms said compensation signal, said compensation circuit having an output coupled to said second combination unit input.

130. The apparatus of claim 129 wherein said compensation circuit further comprises a multiplexer, said multiplexer having a multiplexer output coupled

to said second input of said combination unit, a first multiplexer input that receives said compensation signal, a second multiplexer input that receives a null signal and an input enable coupled to a decode logic output.

131. The apparatus of claim 108 further comprising a level shifter between a clock signal and said second input of said combination unit.

132. The apparatus of claim 131 wherein said clock signal is coupled to the input of a phase detector within a phase lock loop circuit.

133. The apparatus of claim 108 further comprising an amplifier between a clock signal and said second input of said combination unit.

134. The apparatus of claim 133 wherein said clock signal is also coupled to the input of a phase detector within a phase lock loop circuit.

135. The apparatus of claim 108 further comprising a duty cycle circuit between a clock signal and said second input of said combination unit.

136. The apparatus of claim 135 wherein said clock signal is also coupled to the input of a phase detector within a phase lock loop circuit.

137. The apparatus of claim 108 further comprising a circuit that changes frequency of clock signal, said circuit between said clock signal and said second input of said combination unit.

138. The apparatus of claim 137 wherein said clock signal is also presented to the input of a phase detector within a phase lock loop circuit.

139. A method, comprising:

a) receiving a value that corresponds to a desired channel;

b) presenting a control word to a sigma delta modulator based upon said value;

c) forwarding a compensation signal to combination unit if the output signal from said sigma delta modulator is unsuitable for controlling the division within a phase lock loop circuit so that said channel may be received; and

d) combining said compensation signal with said sigma delta modulator output signal to produce a signal that is suitable for controlling the division within a phase lock loop circuit so that said channel may be received.

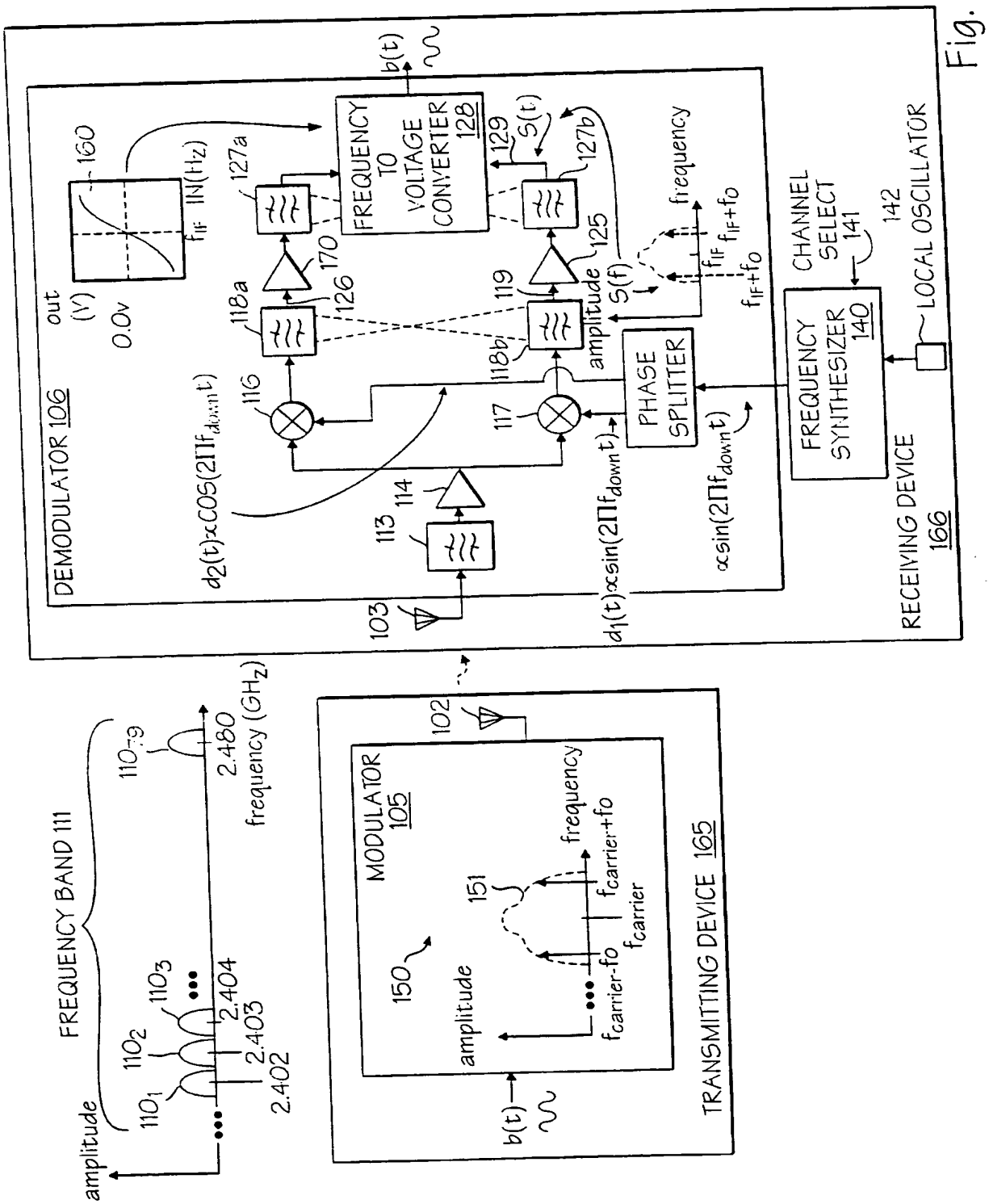
DEMODULATOR 106
RECEIVING DEVICE 166
TRANSMITTING DEVICE 165
MODULATOR 105
FREQUENCY SYNTHESIZER 140
CHANNEL SELECT 141
LOCAL OSCILLATOR 142
PHASE SPLITTER
FREQUENCY TO VOLTAGE CONVERTER 128
FREQUENCY BAND 111
amplitude
frequency
out (V)
0.0v
$f_{IF}$ IN(Hz)
$d_2(t)\propto COS(2\Pi f_{down} t)$
$d_1(t)\propto sin(2\Pi f_{down} t)$
$\propto sin(2\Pi f_{down} t)$
$f_{carrier}$
$f_{carrier}+f_0$
$f_{carrier}-f_0$
$f_{IF}$
$f_{IF}+f_0$
S(f)
S(t)
b(t)
2.402
2.403
2.404
2.480
frequency (GHz)

Fig. 1

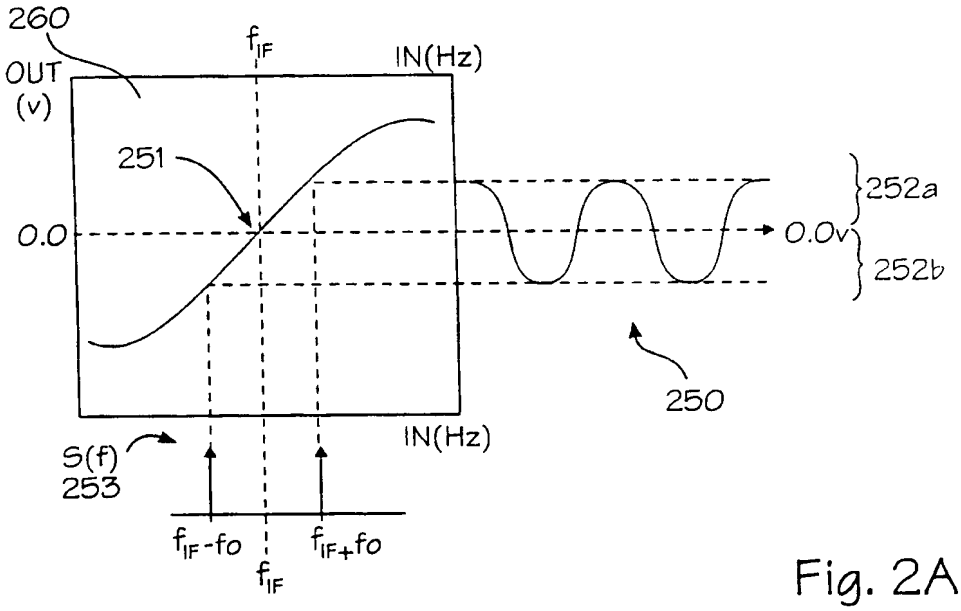
260
OUT
(v)
$f_{IF}$
IN(Hz)
251
0.0
0.0v
252a
252b
250
IN(Hz)
S(f)
253
$f_{IF}$-fo
$f_{IF}$+fo
$f_{IF}$

Fig. 2A

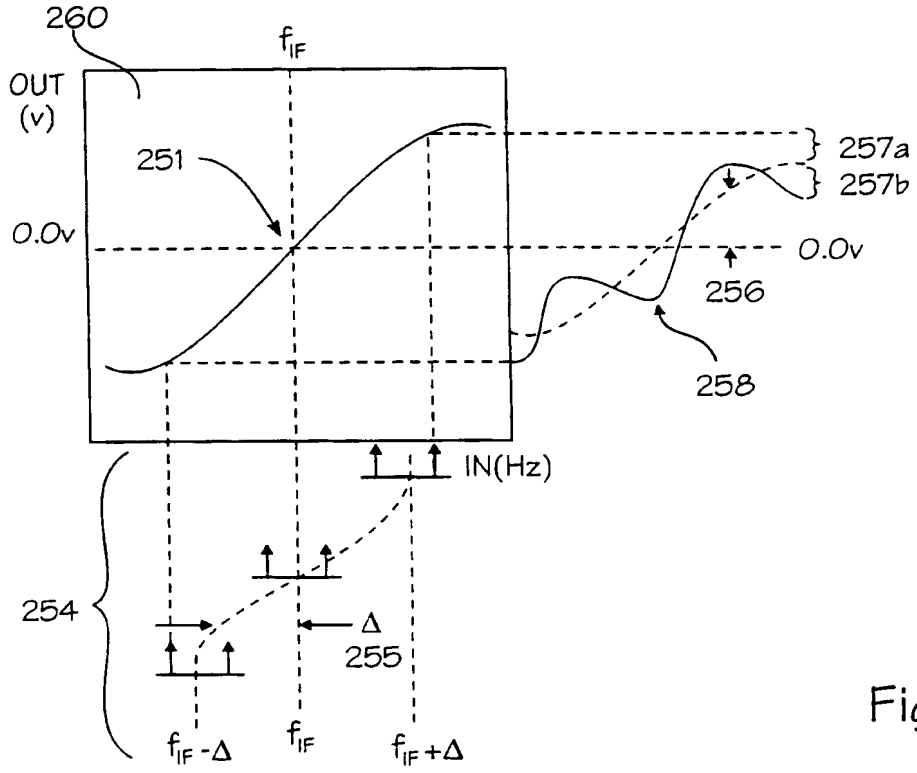
260
$f_{IF}$
OUT
(v)
251
0.0v
257a
257b
0.0v
256
258
IN(Hz)
254
Δ
255
$f_{IF}$ -Δ
$f_{IF}$
$f_{IF}$ +Δ

Fig. 2B

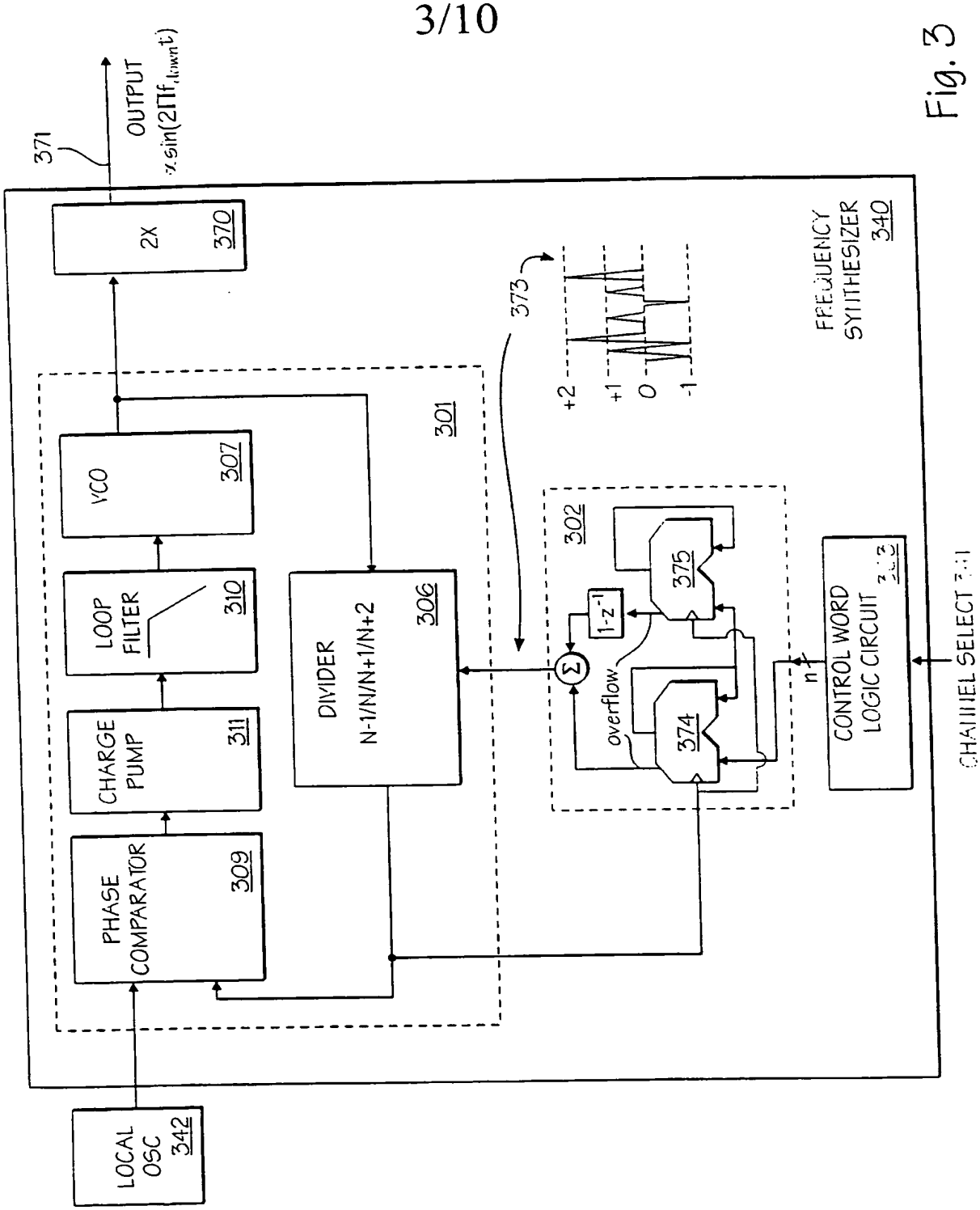
371
OUTPUT
$x\sin(2\Pi f_{down}t)$
2X
370
VCO
307
LOOP FILTER
310
CHARGE PUMP
311
PHASE COMPARATOR
309
301
DIVIDER
N-1/N/N+1/N+2
306
373
+2
+1
0
-1
302
375
1-z⁻¹
overflow
374
n
CONTROL WORD LOGIC CIRCUIT
FREQUENCY SYNTHESIZER
340
CHANNEL SELECT
LOCAL OSC
342

Fig. 3

| | $SDO_{AVE}$ | NAVE =N + $SDO_{AVE}$ for N=92 | $f_{VCO}$ = $f_{osc}$ x $N_{AVE}$ for $f_{osc}$ = 13.000MHz | $f_{DOWN}$ = fVCO x factor for factor = 2 | $f_{carrier}$ = $f_{DOWN}$ + $f_{IF}$ for $f_{IF}$ = 3MHz |
|---|---|---|---|---|---|
| CHANNEL 1 | 0.26923 | 92.26923 | 1.1995 GHz | 2.399 GHz | 2.402 GHz |
| CHANNEL 2 | 0.30769 | 92.30769 | 1.2000 GHz | 2.400 GHz | 2.403 GHz |
| CHANNEL 3 | 0.34615 | 92.34615 | 1.2005 GHz | 2.401 GHz | 2.404 GHz |
| CHANNEL 4 | 0.38462 | 92.38462 | 1.2010 GHz | 2.402 GHz | 2.405 GHz |
| .... | | ... | ... | ... | ... |
| CHANNEL 12 | 0.69231 | 92.69231 | 1.2050 GHz | 2.410 GHz | 2.413 GHz |
| CHANNEL 13 | 0.73077 | 92.73077 | 1.2055 GHz | 2.411 GHz | 2.414 GHz |
| CHANNEL 14 | 0.76923 | 92.76923 | 1.2060 GHz | 2.412 GHz | 2.415 GHz |
| CHANNEL 15 | 0.80769 | 92.80769 | 1.2065 GHz | 2.413 GHz | 2.416 GHz |
| CHANNEL 16 | 0.84615 | 92.84615 | 1.2070 GHz | 2.414 GHz | 2.417 GHz |
| .... | | ... | ... | ... | ... |
| CHANNEL 19 | 0.96154 | 92.96154 | 1.2085 | 2.417 GHz | 2.420 GHz |
| CHANNEL 20 | +1.00000 | 93.00000 | 1.2090 | 2.418 GHz | 2.421 GHz |

Fig. 4

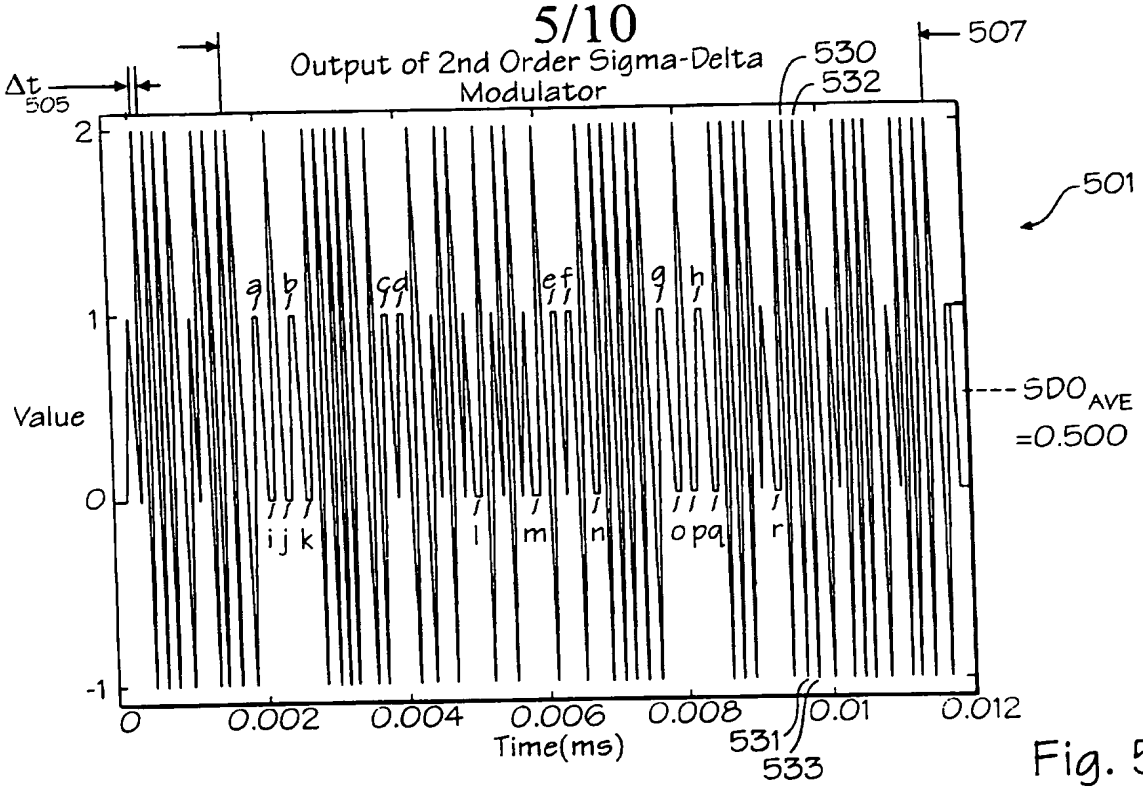
Output of 2nd Order Sigma-Delta Modulator
Δt 505
507
530
532
501
2
1
0
-1
Value
a b c d e f g h
i j k l m n o p q r
SDO AVE =0.500
0 0.002 0.004 0.006 0.008 0.01 0.012
Time(ms)
531
533

Fig. 5A

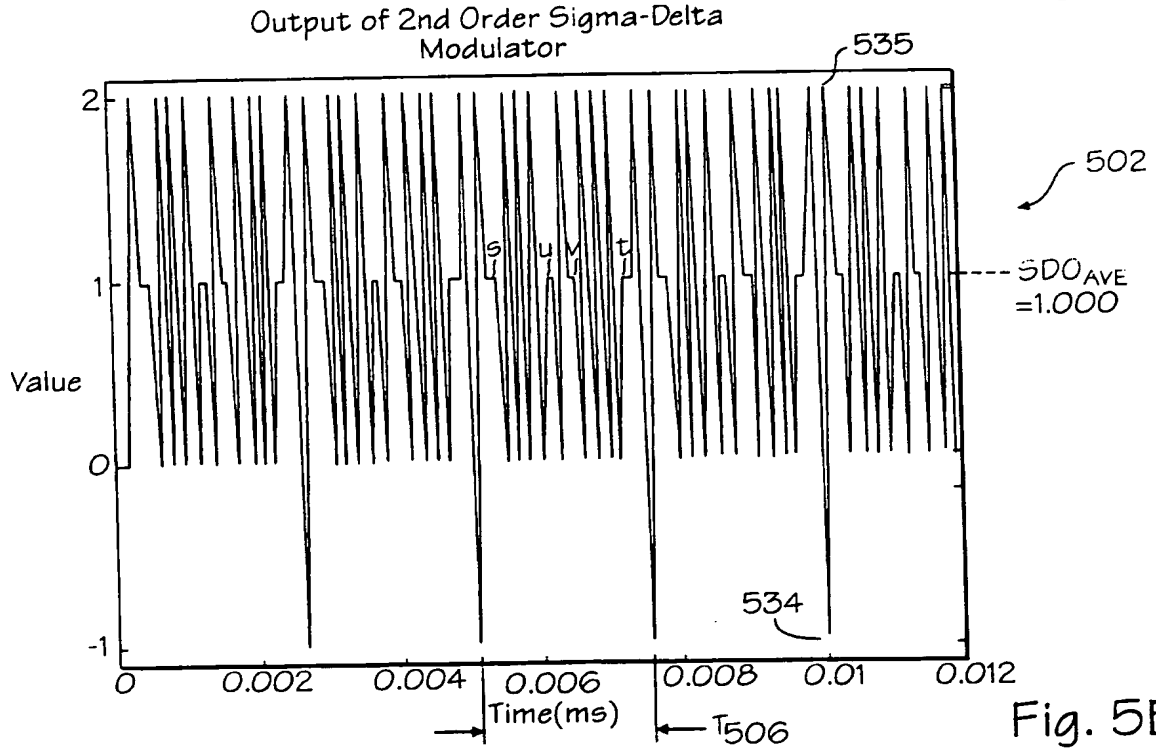
Output of 2nd Order Sigma-Delta Modulator
535
502
2
1
0
-1
Value
s u v t
SDO AVE =1.000
534
0 0.002 0.004 0.006 0.008 0.01 0.012
Time(ms)
T 506

Fig. 5B

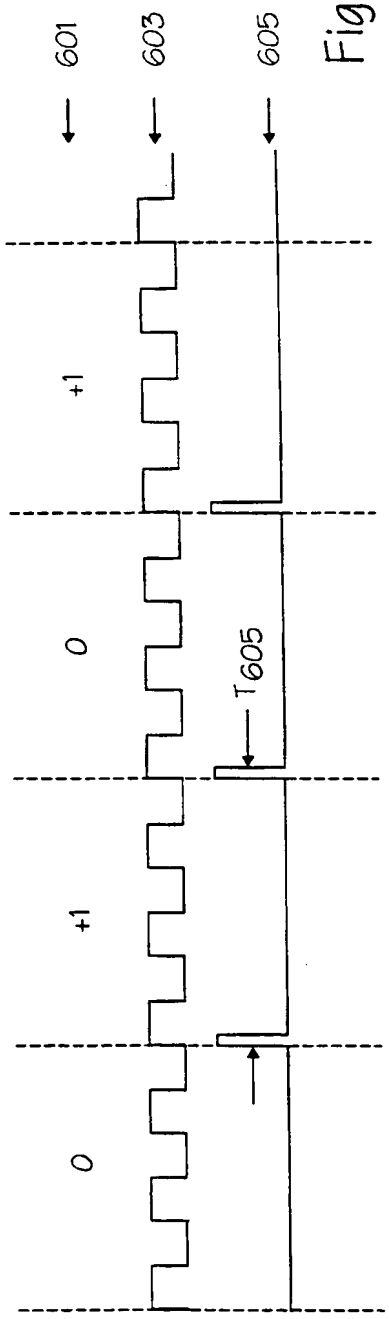


Fig. 6A

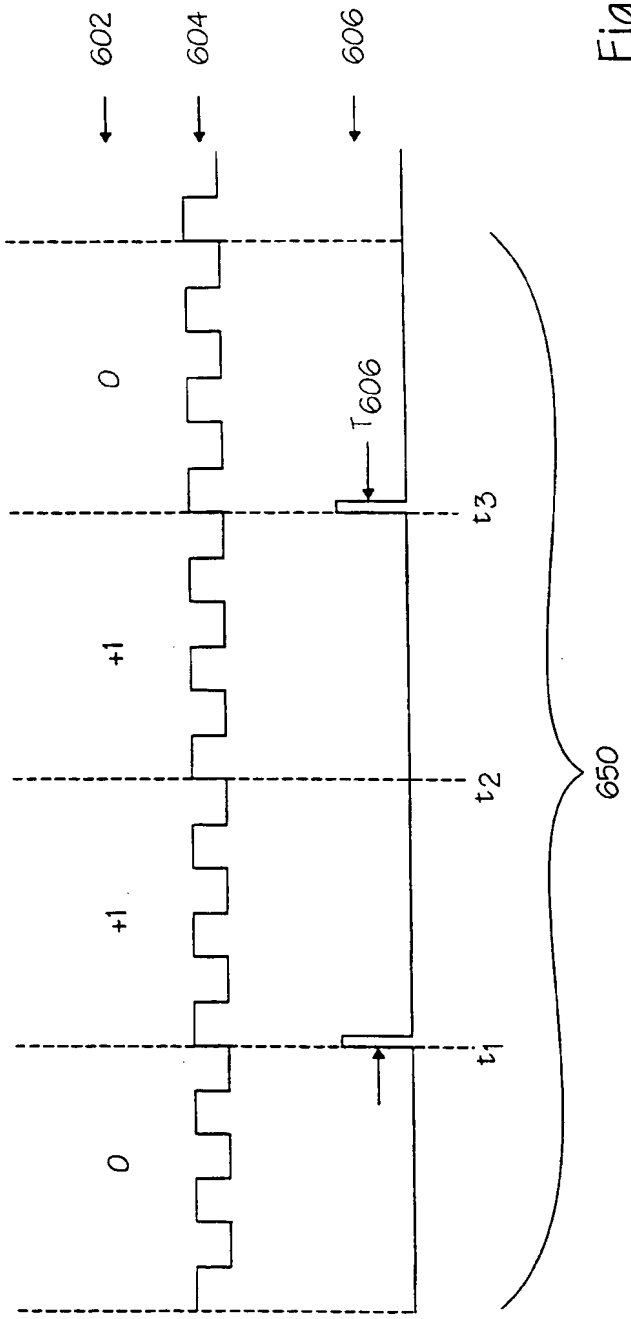


Fig. 6B

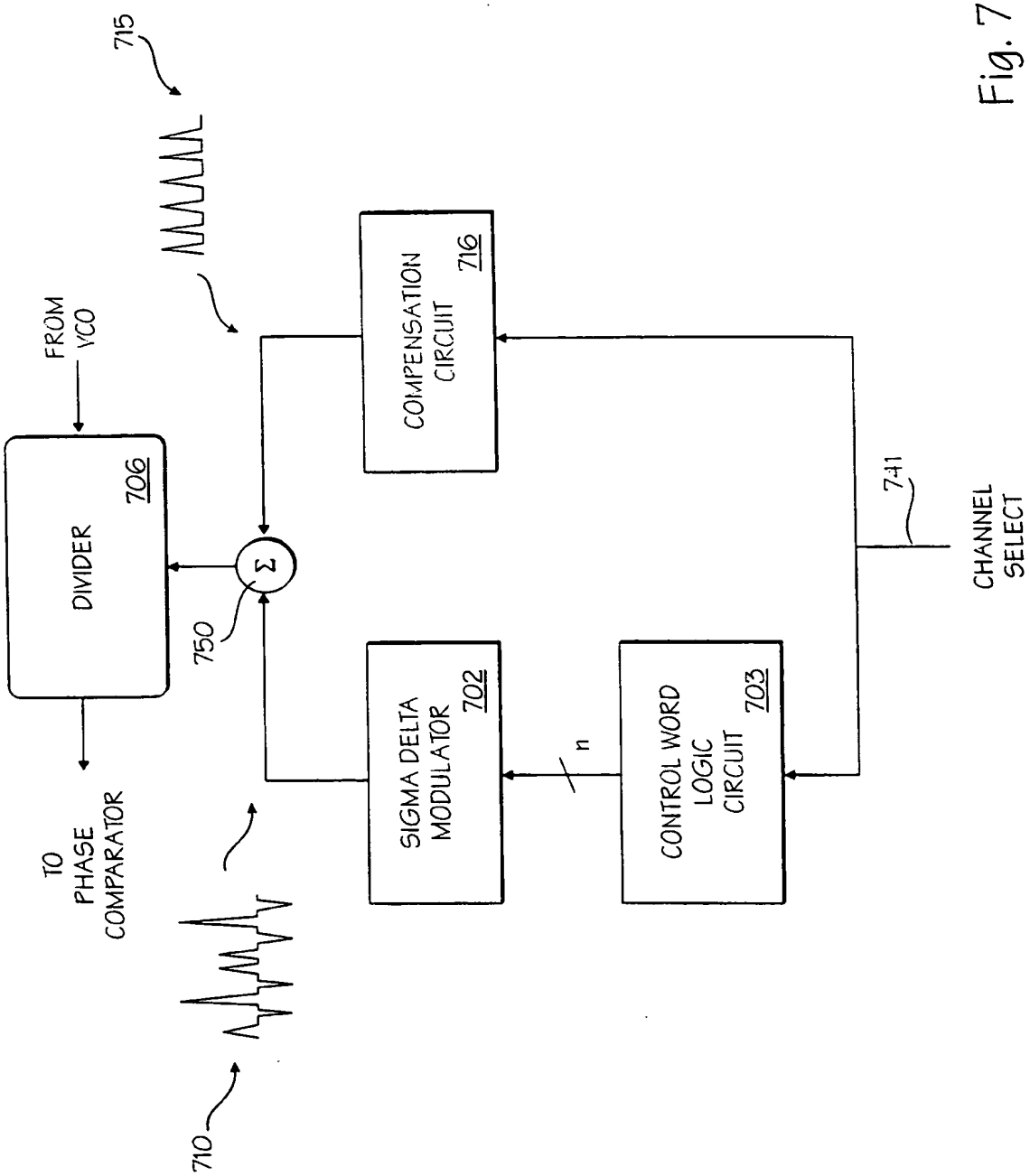
715
FROM VCO
DIVIDER 706
TO PHASE COMPARATOR
710
750
Σ
COMPENSATION CIRCUIT 716
SIGMA DELTA MODULATOR 702
n
CONTROL WORD LOGIC CIRCUIT 703
741
CHANNEL SELECT

Fig. 7

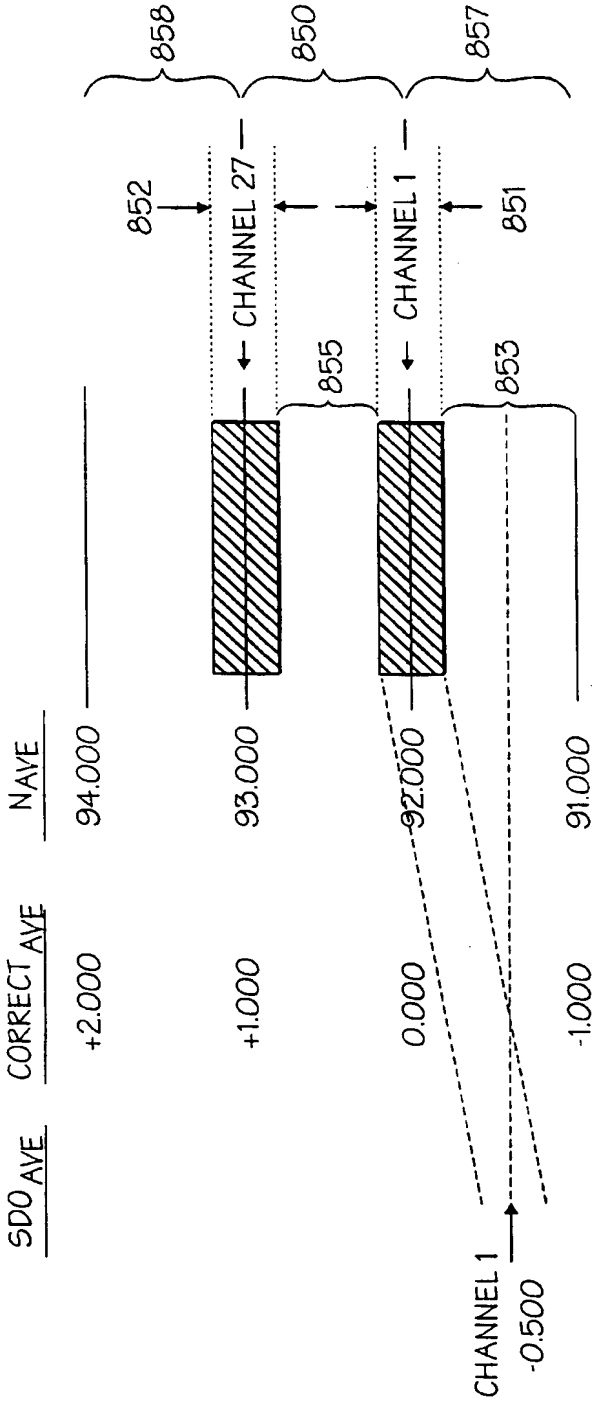
858
850
857
852
CHANNEL 27
CHANNEL 1
851
855
853
NAVE
CORRECT AVE
SDO AVE
94.000
93.000
92.000
91.000
+2.000
+1.000
0.000
-1.000
CHANNEL 1
-0.500

Fig. 8

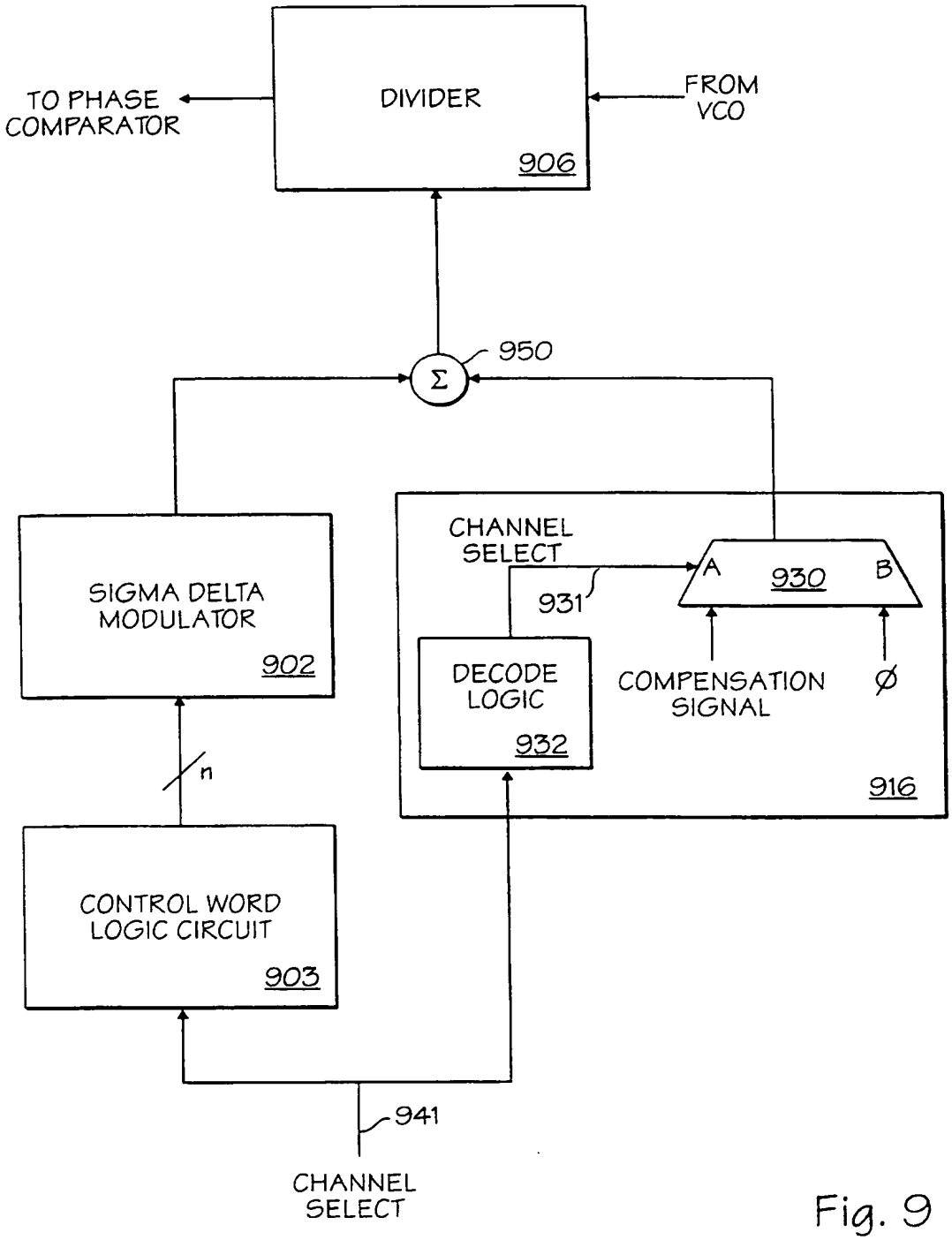
TO PHASE COMPARATOR
DIVIDER
906
FROM VCO
950
Σ
SIGMA DELTA MODULATOR
902
CHANNEL SELECT
931
A
930
B
DECODE LOGIC
932
COMPENSATION SIGNAL
Ø
916
n
CONTROL WORD LOGIC CIRCUIT
903
941
CHANNEL SELECT

Fig. 9

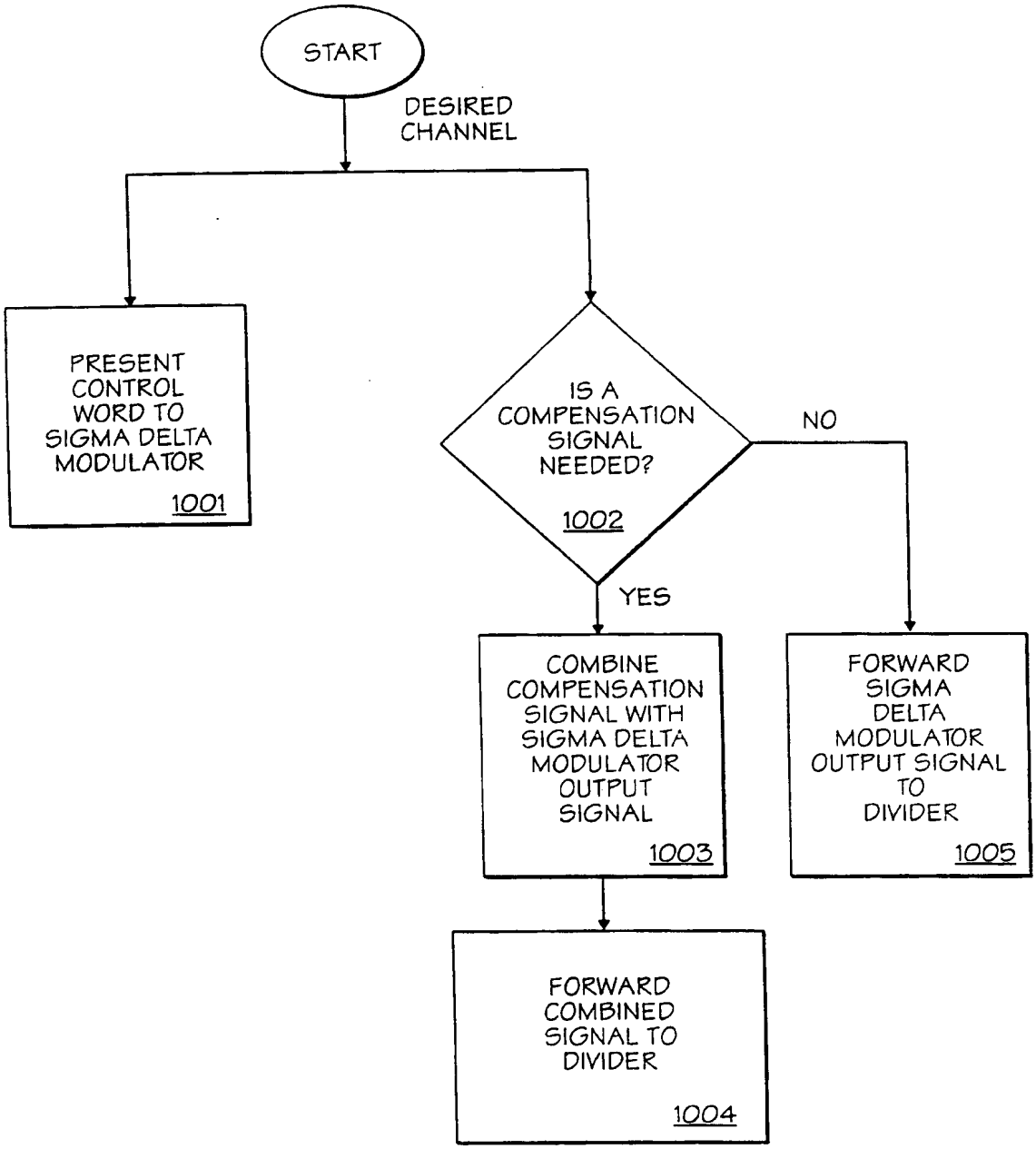
START
DESIRED CHANNEL
PRESENT CONTROL WORD TO SIGMA DELTA MODULATOR
1001
IS A COMPENSATION SIGNAL NEEDED?
1002
NO
YES
COMBINE COMPENSATION SIGNAL WITH SIGMA DELTA MODULATOR OUTPUT SIGNAL
1003
FORWARD SIGMA DELTA MODULATOR OUTPUT SIGNAL TO DIVIDER
1005
FORWARD COMBINED SIGNAL TO DIVIDER
1004

Fig. 10

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/26548

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) :H03D 3/00; H03L 7/18
US CL :375/376; 332/127; 327/105; 455/260;
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 375/247, 376; 332/127, 128; 327/105; 455/260; 341/143

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EAST search terms: divider, sigma delta modulator, compensation, average, frequency synthesizer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A, P | US 6,044,124 A (MONAHAN et al) 28 March 2000, see its entirety. | 1-139 |
| A, P | US 6,047,029 A (ERIKSSON et al) 04 April 2000, see its entirety. | 1-139 |
| A, P | US 6,008,703 A (PERROTT et al) 28 December 1999, see its entirety. | 1-139 |
| A | US 5,834,987 A (DENT) 10 November 1998, see its entirety. | 1-139 |

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

| | | | |
|---|---|---|---|
| * | Special categories of cited documents: | "T" | later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention |
| "A" | document defining the general state of the art which is not considered to be of particular relevance | "X" | document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone |
| "E" | earlier document published on or after the international filing date | "Y" | document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art |
| "L" | document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) | "&" | document member of the same patent family |
| "O" | document referring to an oral disclosure, use, exhibition or other means | | |
| "P" | document published prior to the international filing date but later than the priority date claimed | | |

| | |
|---|---|
| Date of the actual completion of the international search<br>16 NOVEMBER 2000 | Date of mailing of the international search report<br>09 JAN 2001 |
| Name and mailing address of the ISA/US<br>Commissioner of Patents and Trademarks<br>Box PCT<br>Washington, D.C. 20231<br>Facsimile No. (703) 305-3230 | Authorized officer<br>AMANDA T. LE<br>Telephone No. (703)305-4769 |

Form PCT/ISA/210 (second sheet) (July 1998)*